A HIERARCHICAL APPROACH TO TOPOLOGY GENERATION OF ANALOG CIRCUITS

A thesis submitted

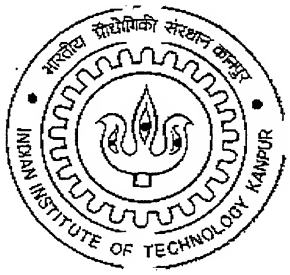
in partial fulfillment of the requirements

For the degree of

MASTER OF TECHNOLOGY

By

RAJARSHI SUR



to the

DEPARTMENT OF ELECTRICAL ENGINEERING
INDIAN INSTITUE OF TECHNOLOGY, KANPUR

APRIL - 2001

14 MAY 2001 /EE
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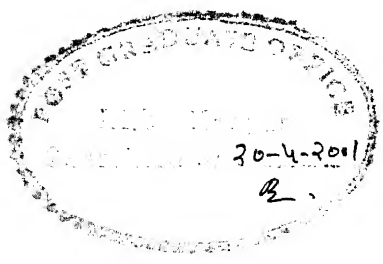

CERTIFICATE

This is to certify that the work contained in the thesis entitled "**A HIERARCHICAL APPROACH TO TOPOLOGY GENERATION OF ANALOG CIRCUITS**" by **Rajarshi Sur** has been carried out under my supervision and that this work has not been submitted elsewhere for the award of a degree.

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ACKNOWLEDGEMENT

I take this opportunity to express my sincere gratitude towards Dr. B. Mazhari without whose guidance this thesis work would have not been in the present form. I am highly grateful to him for his invaluable motivation, encouragement and guidance in making this thesis a success.

I would like to thank Dr. K. Deb, department of ME, for providing me the needed help for my work. I would further like to thank Dr. A. Dutta, Dr. S. Kar, Dr. U. Das, Dr. S. Roy, department of EE whose courses helped me in improving my knowledge.

Last but not the least I would like to thank almighty God, my family members and my friends who had made me reach this stage where I could undertake the work of this magnitude.

Rajarshi Sur

(Rajarshi Sur)

ABSTRACT

The present work describes a hierarchically structured framework for analog circuit synthesis. The analog circuit topologies are represented as a hierarchy of templates of abstract functional sub blocks, each with associated detailed design knowledge. Initially, a particular topology to be designed is selected at the top most level of the hierarchy. This is followed by a design phase where the input specifications are translated from the top most level in the hierarchy to the next lower, more concrete level. Genetic Algorithm based optimization is used during this translation process to obtain the new optimized set of specifications for each of the building sub blocks. The specifications obtained for each sub block are divided into two sets S_0 and S_1. One subset of the specs (S_0) along with the choice of a topology is used to generate a new value for the other subset S_1'. Depending on the match between the elements of S_1 and S_1' the topology is considered a success or a failure. The final topology is selected from among the successful topologies using a suitable figure of merit. The validity of this approach is demonstrated by designing several kinds of 2 stages Miller Compensated op amp which is an affixed connection of different building sub blocks such as load current mirrors, differential pairs, bias current mirrors and trans conductance amplifiers. Detailed SPICE simulations are then performed to verify the results obtained.

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CHAPTER 1
INTRODUCTION

1.1 Introductory Idea

Very large scale integration (VLSI) of devices in IC is now maturing with the current emphasis on deep sub-micron structures and sophisticated innovations, e.g. putting an entire system comprising of digital as well as analog circuits on a single chip, know as System on a Chip (SOC). To match the fast technological trend towards single chip analog/digital VLSI systems, effort has been put worldwide to produce advanced computer aided tools for designing both digital and analog circuits. Architecture and circuit compilation, device sizing, and layout generation are a few familiar tasks on the world of digital IC design, which can be efficiently accomplished by CAD tools. In contrast, the development of tools for designing and producing analog IC's is still at it's primitive stage and lacks the industrial involvement which has already been achieved by their digital counterparts. Thus the design time for mixed analog-digital systems are primarily dominated by the design time of the analog parts [1].

It has been found that in case of a digital design, the basic philosophy that "more is better" i. e the higher the packing density leads to more number of functions in a chip and thus it reduces the cost per function significantly. Most of the digital design is performed at the higher level of abstraction i. e at the system level, using Hardware Description Language (HDL) and then synthesis is carried out followed by the verification. Improvement in design generally leads to working with shortest possible channel length in order to obtain maximum possible packing density and also at the same time optimization of the overall function of the chips. In contrast the motto generally followed in the case of analog design is that "small is beautiful". Here the designers do not stress much on the packing density as it is with the digital design. The devices are not put too close to each other, considering the effects of the parasitic capacitances, which would ultimately deteriorate the performances of the circuit. As a result the focus in circuit design is clearly on the precision usage, and the circuit design is carried out at the transistor level itself. Device geometry is an essential part of the design: specific current

requirements lead to computation of the device sizes. Finally it is found that the "real world" is inherently analog in nature [1].

The main problem of analog synthesis may be defined as the one of selecting the proper topology, sizing the components, and laying out the structure in a manner that realizes the required functionality and meets the desired performance criteria. To fully understand the complexity of analog designs and their automation it is worthwhile comparing the analog and digital design mechanisms [1].

1) In the digital domain, the main performance measures of interests are namely area, power, and delay while for it's counterparts the analog domain the performance interests are numerous and depend on the functional block of interests.

2) The digital signals are generally characterized by two unique states. A impact of these binary discrete levels is that the signal is subjected to formal mathematical treatment using Boolean algebra. On the other hand the analog signals have information in various forms in terms of amplitudes, frequencies, phase differences etc.

3) In the digital domain, system performance may be expressed as a linear function of subsystem performance with little loss of performance accuracy. In the analog domain, system performance is typically a nonlinear function of lower level attributes.

4) With the inclusion of the simple back propagation scheme, digital design methods such as standard cell and the gate array permit layout to be considered independent of circuit topology selection and component sizing. In analog domain, net parasitic capacitances can play a dominant role in determining the high performances of the analog blocks. The use of analog standard cell libraries is not practical due to many divergent performance measures typical of analog systems.

The advent and evolution of computers and digital signal processing methods resulted in a tremendous potential for the processing power, which, in contrast to nature could only process digital signals. Thus the analog interfaces have become very vital and they form the indispensable parts of most of the digital circuits. They provide the

necessary signal conditioning and modification such that they can be processed digitally. These interface circuits vary widely depending on specific functions and applications, such as data acquisition systems, A/D and D/A converters, particle and radiation detector circuits, automotive electronics, biomedical instrumentations, control circuitry, power drivers and many more. Analog circuits are the main signal processors in applications where area, power and high frequency operations are the performances of concern, thus vastly outperforming their digital counterparts. Application specific integrated circuits (ASIC' s) that are designed according to customer specifications therefore are moving rapidly towards SOC [5]. This growing requirements of single-chip mixed VLSI systems, together with the trend towards smaller feature sizes and higher scales of integration, have brought about new dimensions in the circuit design complexity. It has been found that the digital systems have been completely automated by the CAD tools which exploits the hierarchy and structured abstractions. But in contrast the analog design is completely knowledge intensive tasks and analog circuits are still designed by hands by the experts who are familiar with the tradeoffs involved in the performances and IC fabrication processes. CAD tools specifically tailored to analog IC design promise to improve the design process in a variety of ways which are mentioned below [1].

1) By shortening the design time.

2) By simplifying the design process.

3) By improving the likelihood of error-free designs from the first fabrication run.

4) By reducing the design and production cost.

5) By improving the overall manufacturing yield.

6) By allowing easier tracking of the fabrication processes.

7) By retaining the expert design knowledge.

Thus the Analog circuit design is generally achieved through the following steps

1. Topology Selection.

2. Parametric optimization.

3. Layout Generation.

To start with the designer has to select an appropriate topology among the various possible alternatives architectures and topologies available. This is soon followed by assigning the optimized values to the circuit parameters (e. g widths and lengths of MOS transistors, resistors, capacitors, bias voltages and currents etc) which must at the same time satisfy the desired performance criteria. This optimized circuit then needs to be transformed into a layout.

1.2 Literature Review

Research in analog design automation has been relatively slow compared to it' s digital counterpart. By the year 1985, only a handful of analog DA systems were reported and only a few institutions worldwide showed their interests in this field. It is only recently that the research interest in analog DA has been growing dramatically and a plethora of prototype systems, many of which are capable of handling full-custom designs have been reported. The distinction between CAD and DA tools is rather fuzzy in nature and is a debatable one. A CAD tool is a computer based system which provides assistances ranging from merely relieving a designer from long tedious and error prone tasks to performing complete designs with minimal human interventions. The latter class of CAD tools that automate part or the whole of the design process is referred to as DA tools. They are also called silicon compilers. Fig 1.1 depicts schematically a classification of the various analog circuit design approaches.

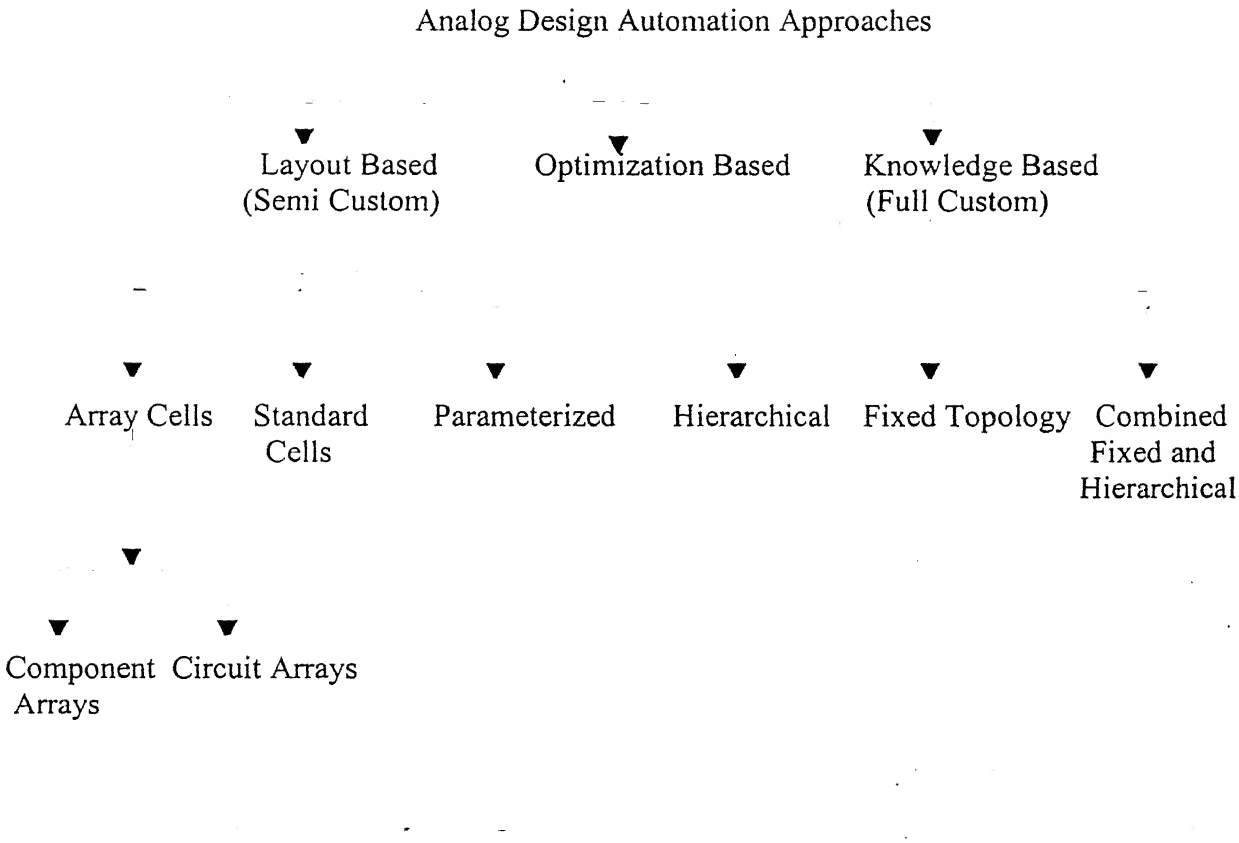

Fig 1.1: Classification of various analog IC design automation approaches.

1.2.1 Layout-Based Design Approach:

With the aim of providing a fast and reliable path to silicon, several systems have been developed that follow a layout-based design approach. In reality, this approach is an adaptation of extensively used standard cell, gate array, and parameterized cell methods found in the digital domain [6]. Since with this approach, designs are controlled to a large extent by layout, it is also referred to as semi-custom bottom-up approach. Analog arrays are pre-designed and laid-out blocks of different sizes, configurations and levels of complexity. The required functions are designed by appropriately programming one or more levels of interconnect. Many such switched-capacitor filter arrays can be fabricated without requiring any external components. Few possible drawbacks are that they do not provide the necessary design flexibility required for high performance analog circuits.

There is a limited range of active and passive components which leads to the design which can be realized only on small discrete points within a vast and continuous performance space. Also at the same time the arrays aren't much cost-effective in terms of silicon usage.

Standard cells address the problem of silicon usage in a better fashion than the arrays. They are actually pre-designed and laid out blocks of varying complexity that reside in the database of the DA system. The required function is implemented by assembling the necessary cells and then by placement and routing. Thus the chips area is also not wasted. This may be implemented successfully in the case of a digital domain but is much restrictive in the analog domain since it is difficult to maintain a rich and a huge database of library of cells. The use of analog parameterized cells is an alternative layout-based design approach. Parameterized cells are similar to the standard cells, but with some additional flexibility gained by allowing some customization of the cells according to the required function [1]. The degree of flexibility provided is directly dependent of the respective module generator-the piece of code that generates the layout of the cell given a set of input parameters.

1.2.2 Knowledge-Based Design Approach

Knowledge-based systems exploit domain knowledge in order to design analog IC's and they address the design task in a full custom way, thereby allowing for maximum flexibility and a potentially better coverage of the circuits performance space. So far the main design philosophies that have evolved and prevailed are the hierarchical and the fixed-topology approaches. The new approach that has evolved from the first two combines some features of both hierarchical and fixed-topology approaches [2].

Hierarchical Approach

The hierarchical design approach has been successfully applied to digital DA and is now seen in analog design also. The main idea involves breaking of the required circuit into smaller distinct parts. Each of these parts is then assigned a set of specifications which, if met then the recombination of these parts will yield the desired circuit performance. The process is repeated in a similar manner for smaller blocks at different

hierarchical levels. The number of such levels depends upon the overall complexity of system. The various systems that use this kind of approach are OASYS [6], BLADES [7], An_Com [19].

Fixed-Topology Approach

This method employs a sizing method in order to compute appropriate sizes for the devices within a given fixed circuit topology. These fixed, un-sized, device level circuit topologies are stored in a knowledge base together with the necessary domain knowledge for dimensioning the devices. The nature of the domain knowledge depends on the method of computing the device sizes. Some of the systems reported in the literature that follow this approach are IDAC [8], OPASYN [9], OAC [10].

Combined Hierarchical and Fixed Topology Approach

There are many knowledge-based design methods, which combine features of both the hierarchical and the fixed topology approaches. This approach is shown as a separate class. ASAIAC [13] is a system which fits into this class of design systems, since it puts together the circuit topology in a hierarchical fashion whereas the design of the individual device dimensions of the topology is performed in a manner that resembles those for fixed topology systems. CAMP [13] is also one such system that designs a circuit first by viewing it as having a fixed topology in order to meet the required performance specifications. ISAID [15] uses the concept of combined hierarchical and fixed topology approach, however it also includes a circuit generator and a circuit corrector. The circuit generator is based on newly developed methods that are used to handle hierarchical generation of topologies. The circuit corrector is an application of qualitative reasoning.

1.2.3. Optimization-Based Design Approach

The optimization based design approach uses recent advances in the optimization theory and algorithms, and relates these to the parametric optimization of analog IC's. The synthesis problem is formulated as one of mathematical programming [3]. The

circuit performances are considered to be the objective functions, which are to be minimized or maximized subject to a set of specification constraints.

Historically, the very first attempt towards analog DA were numerical optimization based. Systems such as DELIGHT.SPICE [16] and ECTASY [13] and the more recent ADOPT [15] consider the sizing of the individual transistors in a given circuit topology as an optimization problem. They employ optimization algorithms, which iteratively adjust the transistor sizes in order to meet the constraints and objectives specified by the user. A simulator is used within the optimization loop to assess the performance of the circuit during the iteration. They are referred to as the simulation based optimization. ASTRX/OBLX [13] developed at CMU also uses this technique. Systems based on numerical optimization techniques are independent of the actual circuit used, the technology and the fabrication process.

But still because of some deficiencies the use of this system has been limited. The circuit designer has to specify a good starting point for the optimization algorithm. A bad starting point may lead to local minimum, potentially rendering a good circuit useless. Specifying constraints and objectives as well as performance measuring procedures is usually a tedious process. Since these systems involve circuit simulation during each iteration within the optimization loop they are slow. In order to avoid the time consuming and expensive simulator inside the optimization loop, several attempts have been made. Once such approach is to adopt simplified but sufficiently accurate models that predict circuit performances and these are used inside the optimization loop. A number of such analytical equation based optimization came out in recent times which use thus technique e. g., OPASYN [9], STAIC [13], FPAD [11], FASY [2]. In OPASYN the parametric optimization is formulated as that for an unconstrained optimization one and is solved using the steepest descent algorithm. The circuit performances are computed using the analytical modeling equations. STAIC features an input modeling language for entering hierarchical circuit descriptions and a numeric solver unit that dynamically integrates analytical model equations. It is also committed to find the global optimum solution and employs a successive solution refinement synthesis methodology.

1.3. Objective

The main objective of our work is to propose a well-defined hierarchically structured framework for analog circuit synthesis. Here the analog circuit topologies are represented as a hierarchy of templates of abstract functional blocks each with associated detailed design knowledge. The hierarchical structure has two important features: it decomposes the design task into a sequence of smaller tasks with uniform structure and it simplifies the reuse of design knowledge. Initially, a particular topology to be designed is selected at the top most level of the hierarchy. This is followed by a design phase where the input specifications are translated from the top most level in the hierarchy to the next lower, more concrete level. Genetic Algorithm based optimization is used during this translation process to obtain the new optimized set of specifications for each of the building sub blocks. The specifications obtained for each sub block are divided into two sets S_0 and S_1. One subset of the specs (S_0) along with the choice of a topology is used to generate a new value for the other subset S_1'. Depending on the match between the elements of S_1 and S_1' the topology is considered a success or a failure. Final topology is selected from among the successful topologies using a suitable figure of merit. In this way we avoid the heuristics based approach which used to appear much frequently in earlier cases. The organization of the thesis is as follows.

Chapter 2 describes the overview of the methodology adopted in this work, e.g., formulation of he problem, the concept of the optimization algorithm which has been utilized in this work.

Chapter 3 describes how each sub blocks namely the load PMOS current mirrors, the bias NMOS current mirrors, the NMOS differential pairs and the trans conductance amplifiers can be represented in terms of its constraints.

Chapter 4 describe how the proposed approach is being used to generate different topologies of Miller compensated dual stages op amp taking into account the various available topologies of different sub blocks which has been discussed in Chapter 3.

The conclusion of work and the scope for future works are discussed in the final Chapter 5.

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CHAPTER 2
HIERARCHICAL STRUCTURED FRAMEWORK

2.1 Introduction

This chapter describes the topology generation which implies both topology selection and the translation process which translate the higher level specifications into specifications for the performance of each sub-block of the topology for cell level analog circuits. An optimization technique is used during this translation phase to obtain the new set of specifications for the different sub blocks. The set of possible topologies of a particular sub block is then found out by verifying whether these new set of specifications are feasible for the design of the sub block. The best and the appropriate topology from the set of possible topologies of the sub-blocks is then selected [6].

For the automation of analog design process all three steps namely topology selection or topology generation, parametric optimization and layout generation have to be automated. Given Fig 2.1 depicts a rough idea about the general analog design procedure.

To date proposed topology selection and topology generation strategies have relied on a limited set of approaches, which can be classified as shown in the Table 2.1 below:

Table 2.1 Classification of different topology selection and generation approaches

	Topology Generation	Topology Selection
Qualitative or heuristics based	OPASYN [9]	FASY [2] STAIC [13] OASYS [6]
Quantitative Approach	PRESENT WORK	PRESENT WORK

It can be seen that most of topology selection and generation approach which have been reported till to date are based on either qualitative statements or on heuristics. Our current work on topology generation which implies topology selection and translation uses the quantitative approach.

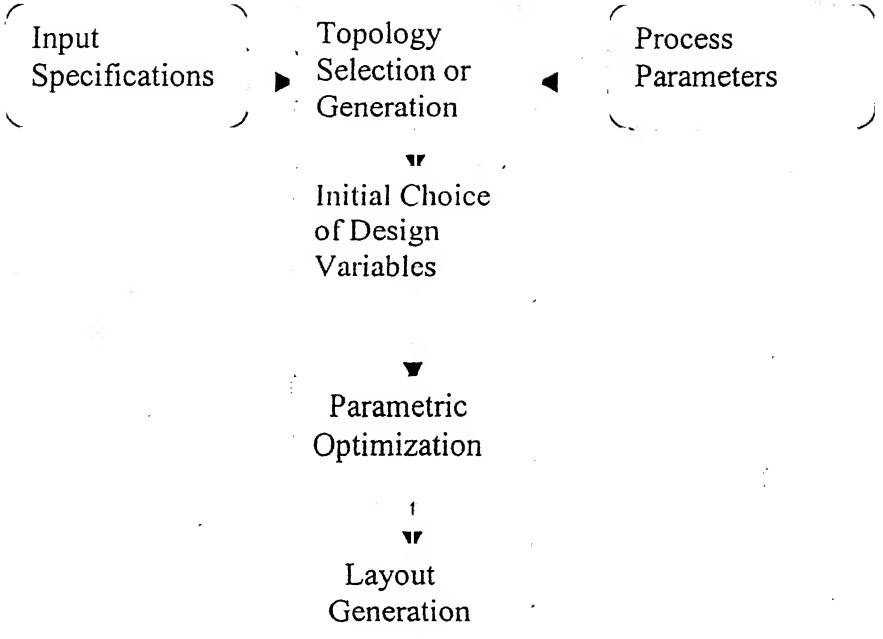

Fig 2.1 General Procedure for Analog Circuit Design

2.2 Framework: Architecture and Implementation

A hierarchically structured framework for analog circuit synthesis is described here. In this work analog circuit topologies are represented as a hierarchy of templates of abstract functional blocks (called design styles) each with associated design knowledge. The framework which is being described is knowledge-intensive in that it relies heavily

on the codification of mature analog design expertise. This framework provides a consistent organization for applying such knowledge to hierarchically designed circuits. Perhaps more importantly, what the framework really demonstrate is the feasibility of attacking tightly coupled analog design problems in a highly stylized, hierarchical fashion. We attack the behavior-to-structure portion of the design task. Our goal is to produce circuit schematics including the device sizes from performance specifications for common analog functional blocks. This approach is motivated by the lack of tools to support the design of custom analog circuits.

In this section we present the framework for organizing the component pieces of a hierarchically structured analog circuit synthesis tool. We begin by outlining the synthesis task, and placing the work in the larger context of framework for automating design. We then describe the central components of the proposed organization: hierarchy, design style selection and translation. Because a critical feature of analog synthesis tasks-one that distinguishes it from better understood digital synthesis tasks-is the nature of analog design knowledge. We also describe the implementation mechanisms for codifying and applying such knowledge in this framework. To understand it better we introduced numbers of simplified hierarchical circuit design example, and use it throughout this section [6].

2.2.1 Overview and Justification

Our intent is to support high-level circuit synthesis for specific classes of analog functions. From an input consisting of detailed performance specifications and process specifications, we need to produce a sized, transistor level circuit schematic. The approach is guided by the design process employed by human designers. Here too we use approximate models for device behavior in order to simplify the analytical formulation of behavior. The final goal is to achieve a good device level topology with correct device sizes to meet all the performance specifications. Numerical optimization tools which employ detailed circuit simulator in an optimization loop may then be applied, if desired, to further fine-tune device sizes based specific goals, e. g performance enhancement. Previous approaches to synthesis have noted the difference between topological design,

which interconnects devices, and sizing, which specifies the performance on individual devices. The proposed framework is based on three critical ideas [6]:

1) Circuit topologies are selected among fixed alternatives; they are not constructed transistor by transistor for each new design. The process of choosing from among these fixed alternatives for the design of a circuit topology is called *design style selection.*

2) The fixed alternatives for circuit topologies are specified hierarchically. A topology for a high level module (e g an A/D converter) is specified as an interconnection of sub-blocks not as an interconnection of transistors. That the topology is fixed implies only that this arrangement of sub-blocks is fixed; the detailed design of individual sub-blocks is also specified here.

3) After selecting a topology to accommodate a set of performance specifications given at one level of the hierarchy, we translate these high level specifications into specifications for the performance of each sub-block of the topology. Informally we are given the behavior of the interconnected sub-blocks taken as a whole, and we must deduce the specifications for each sub-block required to achieve this overall behavior. Device sizing, in the conventional sense, occurs when this process of translation reaches the bottom of the hierarchy and specifies the behavior of individual transistors.

A hierarchical representation makes the synthesis task more tractable, but has one disadvantage. By recasting circuit design as a sequence of alternating topology selection and translation steps, we loose the easy ability to implement design tricks that jump across many levels of the hierarchy. Thus we loose a flattened view of the design in which all details of individual devices are simultaneously exposed, and independently changeable. Expert designers often employ such tricks to push circuits close to the limits of the available performance (simultaneously exploiting tricks involving topologies, sizing, layout and process.). Since the hierarchical explicitly prevents the design plan for one module from depending on the details of how other modules are implemented, our approach may not be able to reach such extremal points in the design space of a given block.

The two-step topology selection and translation process is illustrated for an abstract block in Fig 2.2. A particular topology is chosen because it is the best candidate

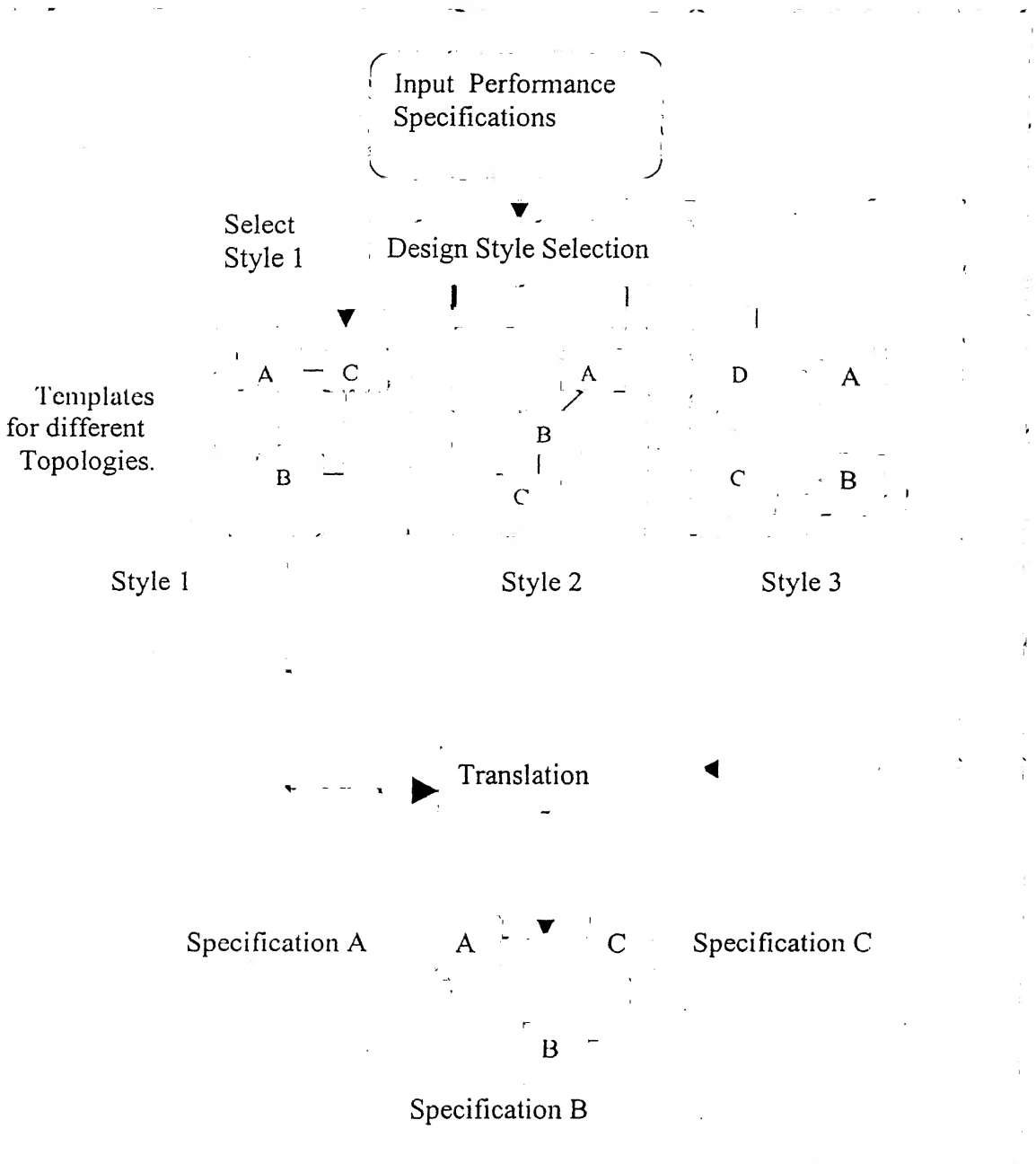

Fig 2.2 Topology Selection and Translation Process

to match the specified block-level behavior; the translation step then decides how it's sub-blocks must behave to meet the block-level specifications. Restricting the design of sub-block interconnections to a choice among fixed alternatives allows us to concentrate

on specifying the electrical characteristics of the connected sub-blocks. A hierarchical representation of topologies vastly simplifies the translation task because it tends to reduce the number of sub-blocks and simplify their connections; it is generally easier to synthesize the specifications for five connected blocks then to synthesize individual parameters for each of 50 connected transistors. Hierarchy also simplifies the selection task, because we do not require a vast number of nearly identical topologies differing only in low-level design styles in the hierarchy actually specify transistors.

2.3 Topology Description

To carry out topology selection, the following requirements must be met.

1) Each topology needs to be described in such a manner that it is easy to distinguish it from other alternative topologies.

2) The specifications or some function of them must be used as the topology selection criterion.

3) The selection criterion chosen above must be related to the topology description in a simple and explicit manner.

In the present work, a topology is characterized by a set of equations which describe the input specifications in terms of the device characteristics. All the information, which is traditionally described in terms of statements, is embedded in these analytical equations. It has been explained briefly in the Fig 2.3 shown. The advantage of this present approach is that technology dependent parameters are represented symbolically and can by easily modified. Therefore while this new description includes within it all the information that is traditionally presented in the form of qualitative statements, it also offers the advantage of being precise.

2.3.1 Mechanisms to support Topology Selection:

In this work, each circuit block is allowed to have different styles, where a style is just a different interconnection of lower level building blocks. For example there is only one block called "op amp" in this work, but it is available in different circuit styles: Simple operational trans-conductance amplifier (OTA), Miller-compensated dual stage op amp, Folded cascade op amp. Each of these styles is not a transistor schematic: rather

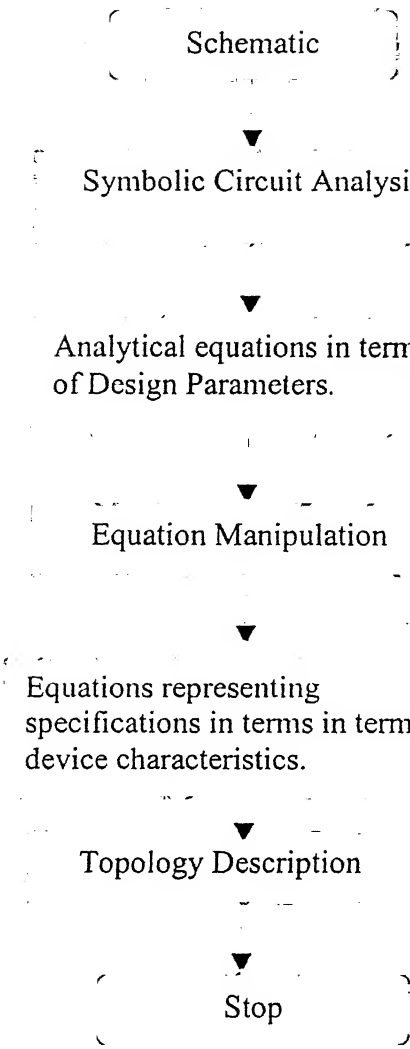

Fig 2.3 Topology Description

it is an interconnection of lower level blocks like load stage current mirrors, differential pairs, bias stage current mirrors and trans-conductance amplifiers. Before we can invoke the translation process to refine op amp specifications into the current mirrors, differential pair etc., specially, we must select one of these op amp styles. Selection happens at all levels of the hierarchy. For example, mirrors, differential pairs, and trans-conductance amplifiers all come in various styles as well, although now the sub-blocks in

each of these styles are actually transistors. In the present work we have implemented only the Miller compensated dual stage op amp for detailed analysis

2.3.2 Mechanisms to support Translation:

Translation involves knowledge of how performance specifications for a high-level block should be transformed into specifications for each sub-block. As an example we have considered the Miller compensated dual stage op amp. At this level of design we have no details of the transistor-level design of this op amp. The op amp appears as affixed connection of building blocks such as load current mirrors, differential pairs, bias current mirrors and trans-conductance amplifiers. To get to the transistors, we will use two levels of translation: first op amp performance specifications will be used to design the sub-blocks; second, the (new) specifications for each sub block will be used to design the transistors that comprise each of the sub-blocks. It is important to recognize that "to design" in this translation process mean "to produce performance specifications for". The output of this translation task is a set of designed sub-blocks, specifically, a set of input specifications for each of these sub-blocks. The process then repeats inside each sub-block. Thus the implementation of the translation tasks in the overall framework can be summarized as follows:

1) Topologies i. e, design styles, are implicitly represented as statically stored templates of connected sub-blocks.

2) The process by which a high-level block specification is translated into sub-block specifications is implemented-albeit rather loosely in the style of a planning system. A design plan is associated with each fixed topology and executed when the topology is instantiated.

Because we view block-level topologies as static templates we can easily represent all relevant, useful circuit relationships within the design plan for the template, for use during the translation step.

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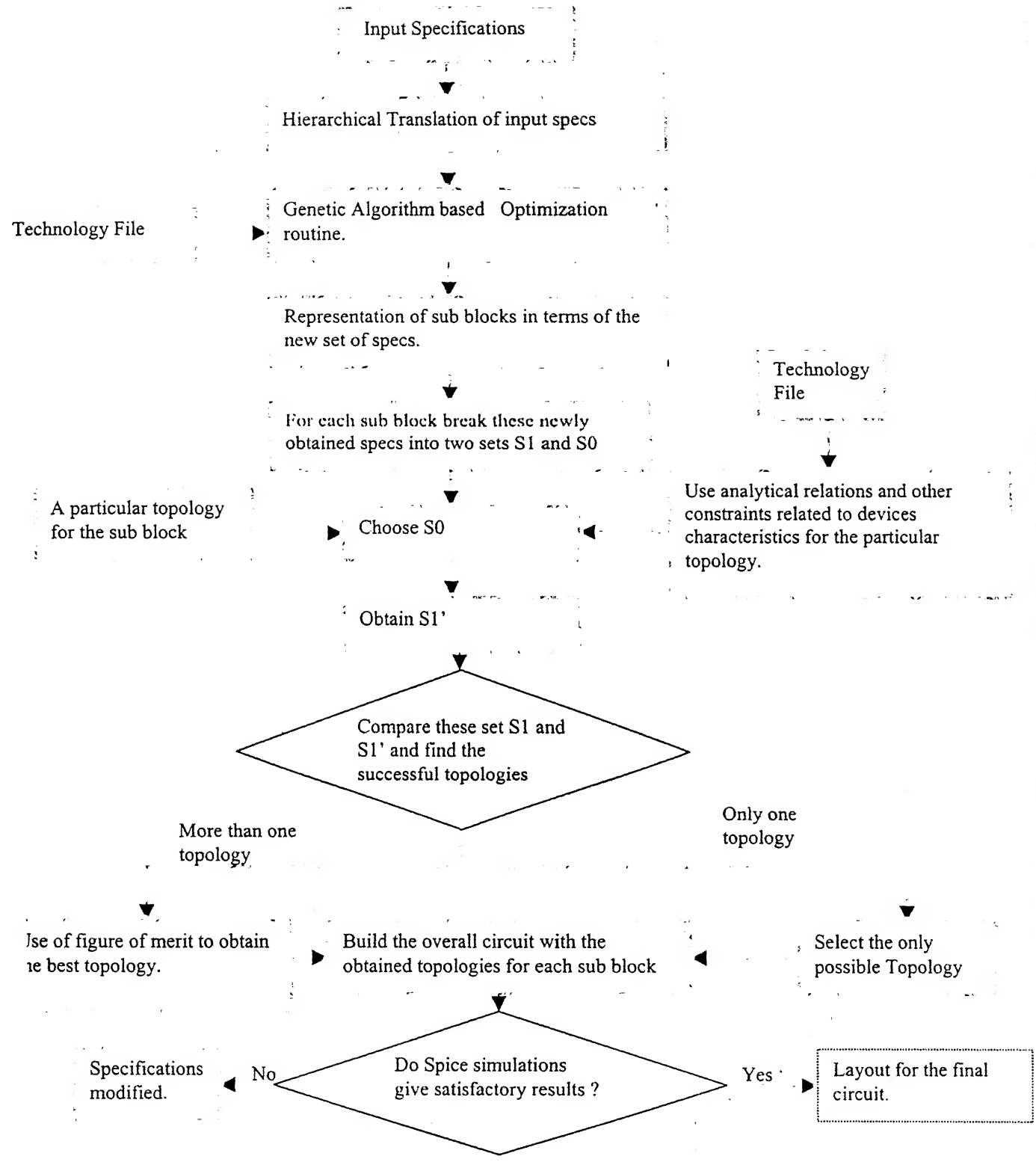
Input Specifications
Hierarchical Translation of input specs
Technology File
Genetic Algorithm based Optimization routine.
Representation of sub blocks in terms of the new set of specs.
Technology File
For each sub block break these newly obtained specs into two sets S1 and S0
A particular topology for the sub block
Choose S0
Use analytical relations and other constraints related to devices characteristics for the particular topology.
Obtain S1'
Compare these set S1 and S1' and find the successful topologies
More than one topology
Only one topology
Use of figure of merit to obtain the best topology.
Build the overall circuit with the obtained topologies for each sub block
Select the only possible Topology
Specifications modified.
No
Do Spice simulations give satisfactory results ?
Yes
Layout for the final circuit.

2.3.3 Final Topology Selection

Initially, a particular topology to be designed is selected at the top most level of the hierarchy. This is followed by a design phase where the input specifications are translated from the top most level in the hierarchy to the next lower, more concrete level. Genetic Algorithm based optimization is used during this translation process to obtain the new optimized set of specifications for each of the building sub blocks. The specifications obtained for each sub block are divided into two sets S_0 and S_1. One subset of the specs (S_0) along with the choice of a topology is used to generate a new value for the other subset S_1'. Depending on the match between the elements of S_1 and S_1' the topology is considered a success or a failure. Final topology is selected from among the successful topologies using a suitable figure of merit. In this way we avoid the heuristics based approach

2.4 Optimization

Many real world search and optimization problems involve inequality and/or equality constraints and are thus posed as constrained optimization problems. In trying to solve constrained optimization problems using genetic algorithm (GA's) or classical optimization methods [26], penalty function methods [26] have been the most popular approach, because of their simplicity and ease of implementation. However since the penalty function method is generic and is applicable to any type of constraint (linear or nonlinear), their performance is not always satisfactory. Thus researchers have developed sophisticated penalty functions specific to the problem at hand and the search algorithm used for optimization. However the most difficult aspect of the penalty function approach is to find appropriate penalty parameters needed to guide the search towards the constrained optimum. Here we have used GA's population based approach and ability to make pair wise comparison in tournament selection operator are exploited to devise a penalty function approach that doesn't require any penalty parameter. Careful

comparisons among feasible and infeasible solutions are made so as to provide a search direction towards the feasible region. Once sufficient feasible solutions are found a niching method along with a controlled mutation operator is used to maintain diversity among feasible solutions. This allows a real parameter GA's crossover operator to continuously find better feasible solutions, gradually leading the search near the true optimum solutions.

2.4.1 Problem Formulation:

In Multi-objective evolutionary algorithms which use non-dominated sorting and sharing have been mainly criticized for their (i) $O(MN^3)$ computational complexity (where M is the number of objectives and N is the population size), (ii) non-elitism approach, and (iii) the need for specifying a sharing parameter. Here we have used non-dominated sorting based multi-objective evolutionary algorithm called Non-Dominated Sorting GA-II or NSGA-II [29] which alleviates all the above three difficulties. Simulation results have soon that the NSGA-II is able to find much better spread of solutions and better convergence near the true Pareto-optimal front. The different module which form parts of NSGA-II are as described below:

2.4.2 Fast Non-Dominated Sorting Approach:

In this approach, every solution form the population is kept in a set *P'*. Thereafter each solution *p* (the second solution onwards) is compared with all members of the set *P'* one by one. If solution *p* dominates any member *q* of *P*, then the solution *q* is removed from *P'*. This way nonmembers of the non-dominated front get deleted from *P'*. Otherwise, if solution is *p* is dominated by may member of P', the solution p is ignored. If solution *p* is not dominated by nay member of *P'*, it is entered in *P'*. This is how the set *P'* grows with non-dominated solutions. The all the solutions of the population is checked, the remaining members of *P'* constitute the non-dominated set..

P' = find non-dominated-front(*P*)

P' = {1} include first member in *P'*

For each $p \in P \wedge q \notin p$ take one solution at a time

$P' = P' \cup \{p\}$	include p in P' temporarily
for each $q \in P' \wedge q \neq p$	compare p with other members of P'
if $p < q$, then $P' = P' \setminus \{q\}$	if p dominates a member of P', delete it
else if $q < p$, then $P' = P' \setminus \{p\}$	if p is dominated by other members of P', do not include p in P'.

To find other fronts, the members of P' will be discounted from P and the above procedure is repeated, as outlined.

F = fast non dominated-sort (P)	F is a set of non-dominated fronts
$i = 1$	i is the front counter and is initialized to one
until $P \neq \phi$	
F_i = find non-dominated front (P)	find the non-dominated front
$P = P \setminus F_i$	remove the non-dominated solutions from P
$i = i + 1$	increment the front counter

At the end of this operation, solutions of the first non-dominated front are stored in F_1, solutions of the second non-dominated front are stored in F_2, and so on.

2.4.3 The Main Loop:

Initially, a random parent population P_0 is created. The population is sorted based on non-domination. Each solution is assigned a fitness (or rank) equal to its non-domination level (1 is the best level, 2 is the next-best level and so on). Thus, minimization of fitness is assumed. At first the usual binary tournament selection, crossover and mutation operators are used to create a child population Q_0 of size N. Since elitism is introduced by comparing current population with previously- found best non-dominated solutions, the procedure is different after the initial generation.

$R_t = P_t \cup Q_t$	combine parent and children population

$P' = P' \cup \{p\}$	include p in P' temporarily
for each $q \in P' \wedge q \neq p$	compare p with other members of P'
if $p < q$, then $P' = P' \backslash \{q\}$	if p dominates a member of P', delete it
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$R_t = P_t \cup Q_t$	combine parent and children population

F = fast-non-dominated-sort(R_t)	$F = (F_1, F_2, \ldots\ldots)$, all non-dominated fronts of R_t.
$P_{t+1} = \Phi$ and $i = 1$	
until $P_{t+1} + F_i \leq N$	till the parent population is filled
$P_{t+1} = P_{t+1} \cup F_i$	include i-th non-dominated front in the parent pop
$i = i + 1$	check the next front for inclusion
Sort (F_i, <n)	sort in descending order using <n
$P_{t+1} = P_{t+1} \cup F_i[1: N - P_{t+1}]$	choose the first $(N - P_{t+1})$ elements of cal F_i
Q_{t+1} = make-new-pop (P_{t+1})	use selection, crossover and mutation to create a new population Q_{t+1}
$t = t+1$	increment the generation counter

2.4.4 Constraints Handling Approach:

Here the constraint handling method uses the binary tournament selection, where two solutions are picked from the population and the better solution is chosen. In presence of constraints, each solution can be either feasible or infeasible. Thus there may be at most three situations: (1) both solutions are feasible, (2) one is feasible and the other is not, and (3) both are infeasible. For single objective optimization, we used a simple rule for each case:

Case (1) Choose the solution with better objective function value.

Case (2) Choose the feasible solution.

Case (3) Choose the solution with smaller overall constraint violation.

Since in no case constraints and objective function values are compared with each other, there is no need of having any penalty parameter, a matter which makes the constrained handling approach much attractive.

In the context of multi objective optimization, the later two cases can be used as they are, and the first case can be resolved by using the crowded comparison operator as

F = fast-non-dominated-sort(R_t)	$F = (F_1, F_2, \ldots\ldots)$, all non-dominated fronts of R_t.
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In the context of multi objective optimization, the later two cases can be used as they are, and the first case can be resolved by using the crowded comparison operator as

before. To maintain the modularity in the procedures of NSGA-II the definition of domination between two solutions i and j has been modified:

Definition: *A solution is said to constrained-dominate a solution j, if any of the following conditions is true:*

1) Solution i is feasible and solution j is not.

2) Solutions i and j are both infeasible, but solution i has a smaller overall constraint violation.

3) Solutions i and j are feasible and solution i dominates solution j.

The effect of using this constrained-domination principle is that any feasible solution has a better non-domination rank than any infeasible solution. All feasible solutions are ranked according to their non-dominance level based on the objective function values. But, between two infeasible solutions, the solution with a smaller constraint violation has a better rank.

2.5 Specification Modification

In some cases we find that even after obtaining the optimized specifications the various topologies of each sub block find it impossible to satisfy this set of new specifications. Then the modification of the input performance specifications becomes necessary while proceeding ahead with this design methodology. The modification of the specifications requires some good heuristics knowledge of circuit topologies and also knowledge about the approximate values of performance specifications achieved by it. The present description of topologies of a particular sub-block in terms of its device characteristics is very useful for specification modifications also.

CHAPTER 3
BASIC ANALOG CIRCUITS

3.1 Introduction

In our work we have considered the design of Miller Compensated dual stage op amp. At the top most level we don't have any details of the transistors level design of this op amp. The op amp appears as affixed connection of building blocks such as load current mirrors, differential pairs, bias current mirrors and trans conductance amplifiers. Each such sub block can be represented by different possible topologies. A brief description of the different possible topologies available for each sub block is given in this chapter. Fig 3.1 illustrates how a simple 2 stage Miller compensated op amp can be hierarchically broken down into sub blocks of current mirrors, differential pairs and trans conductance amplifiers.

3.2 Current Mirror

The current mirror, also referred to as current source/sink, is the most basic building block in CMOS IC design and is used in various analog circuits. Ideally the output impedance should be infinite and it should be capable of supplying and drawing a constant current over a wide range of voltage across it. However in reality the performance of all practical current mirrors is limited by finite values of output impedance and small output voltage swing. Depending on the requirements a particular current mirror is chosen keeping in mind the performance it can provide. The following types of current mirrors are designed and have been used quite extensively in our work.

1. Simple Current Mirror.
2. Cascode Current Mirror.
3. Wilson Current Mirror.

For the design of current mirrors, the performance objectives are to minimize the total area, presence of a large output impedance for a given current and more or less constant current for an output voltage range specified by the designer.

Table 3.1 Performance specification of Current Mirror

Sl. No	Symbol	Specification	Typical objective
1	I_{out}	*Output current*	*User specified*
2	$Vout_{min}$	*Minimum out voltage*	*Minimize*
3	R_{out}	*Output resistance*	*Maximize*
4	*AREA*	*Active Area*	*Minimize*

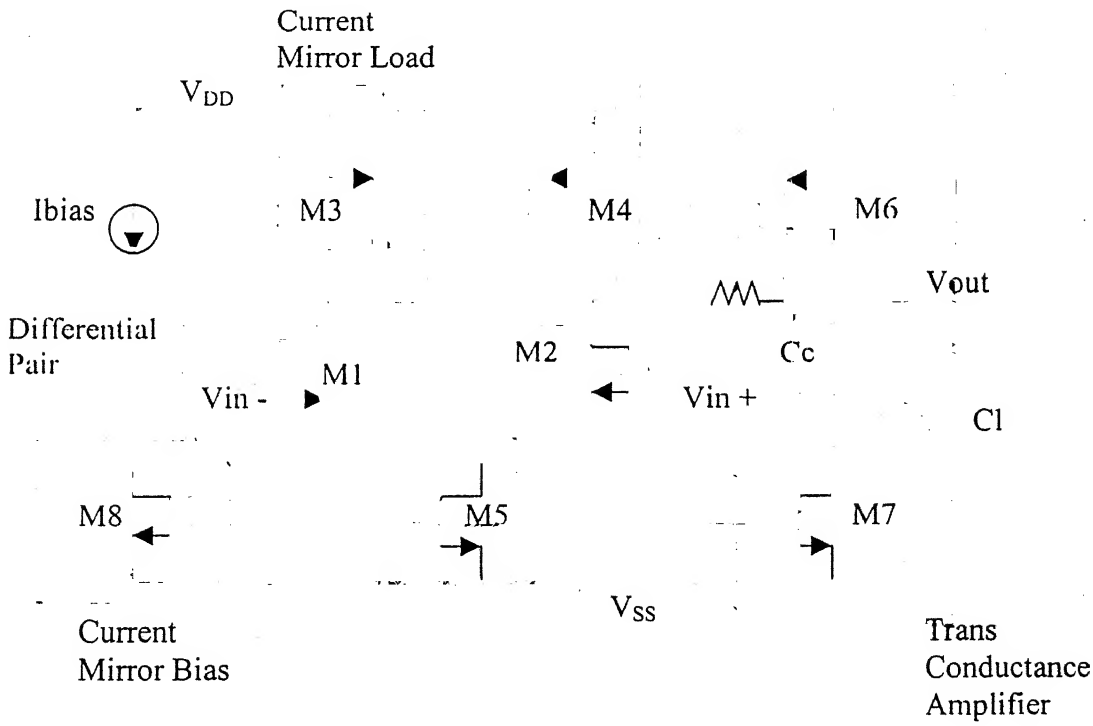

Fig 3.1 General Hierarchical model of a simple 2 stage Miller compensated op amp

In our work the current mirrors would be used in the biasing as well as in the load stage of a Simple 2 stage Miller Compensated op amp. Below given are the detailed

explanations about the current mirrors which are used as load as well in the biasing stage. We are using the NMOS current mirrors which act as the biasing stage and PMOS current mirrors which acts as the active load stage for a Simple 2 stage Miller Compensated op amp.

3.2.1 Simple Current Mirror

The schematics of NMOS simple current mirror and PMOS simple current mirror are shown below in Fig 3.1.1 and Fig 3.1.2. For a simple current mirror it has been assumed that both the transistors M1 and M2 have the same dimensions. The bias current (I_{bias}) is thus reflected as output current (I_{out}). The mathematical relations that relate the performance specifications to the device characteristics are discussed below.

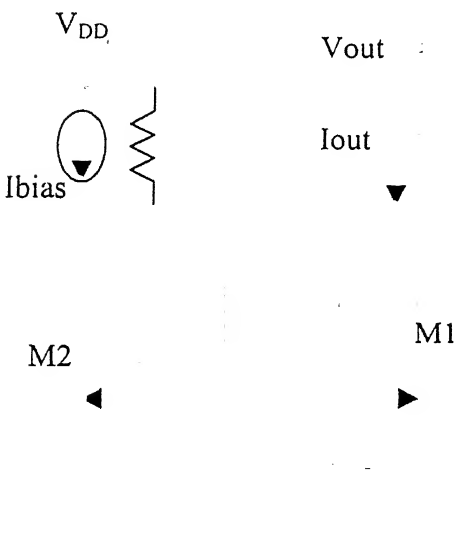

Fig 3.1.1 NMOS Simple CM

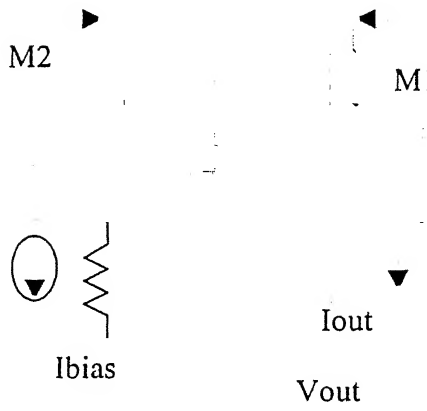

Fig 3.1.2 PMOS Simple CM

The output impedance is (*Ros*) is given by:

$$Ros = ro_1 = \frac{1+\lambda\, Vds1}{\lambda\, Ids1} \qquad (3.1)$$

where *Ids1* is the drain to source current of M2 and equal to the output current (*Ios*). *Vds1* is the same as the output voltage *(Vos)*.

The minimum output voltage $(Vout_{min})$ is given by:

$$Vos = Vout_{min} = |Vgs_1| - |Vt_o| \quad (3.2)$$

The overall active area is given by:

$$AREA = 2 \times W \times Lmin \quad (3.3)$$

The equations mentioned above can be manipulated to obtain a set of equations which depicts the specifications of a SCM in terms of its constraints. These set of equations are mentioned below separately for a NMOS simple current mirror (SCM) and a PMOS SCM. For an NMOS SCM the set of equations are:

$$Ros = \frac{1 + \lambda n \Delta V1}{\lambda n Ios}$$

$$Vo_{min} = \Delta V1 + Vss$$

$$Area = Ld^2 \left[\frac{4Ios}{kn' \Delta V1^2 (1 + \lambda n \Delta V1)} \right]$$

For a PMOS SCM the set of equations are :

$$Ros = \frac{1 + \lambda p \Delta V1}{\lambda p Ios}$$

$$Vo_{min} = V_{DD} - \Delta V1$$

$$Area = Ld^2 \left[\frac{4Ios}{kp' \Delta V1^2 (1 + \lambda p \Delta V1)} \right]$$

$\Delta V1$ is the gate overdrive which is given by:

$\Delta V1 = |Vgs| - |Vto|$ where Vto is the threshold voltage for a MOS transistor at zero body-source voltage.

3.2.2 Cascode Current Mirror

The cascode current mirror is a combination of two simple current mirrors. The cascode current mirror is generally used to improve the overall output impedance of the current mirror. The schematics for a NMOS and PMOS cascode current mirror (CCM) are shown below in Fig 3.2.1 and Fig 3.2.2. Assuming the dimensions of M1 is same as M2 and also M3 is same as M4 the mathematical expression which relate the performance specifications to the different device characteristics are given below:

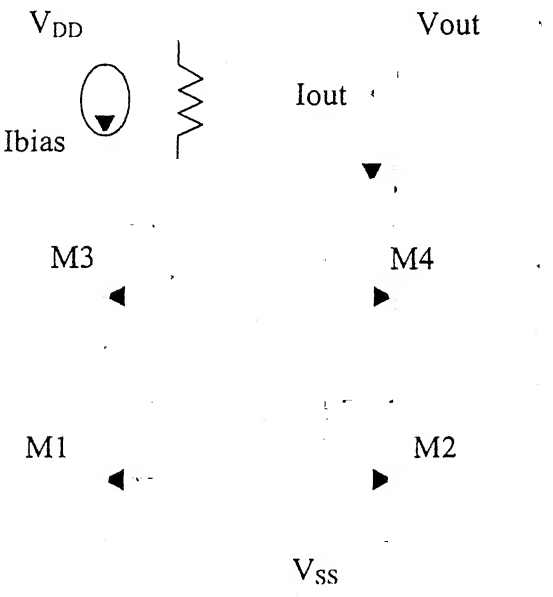

Fig 3.2.1 NMOS Cascode CM

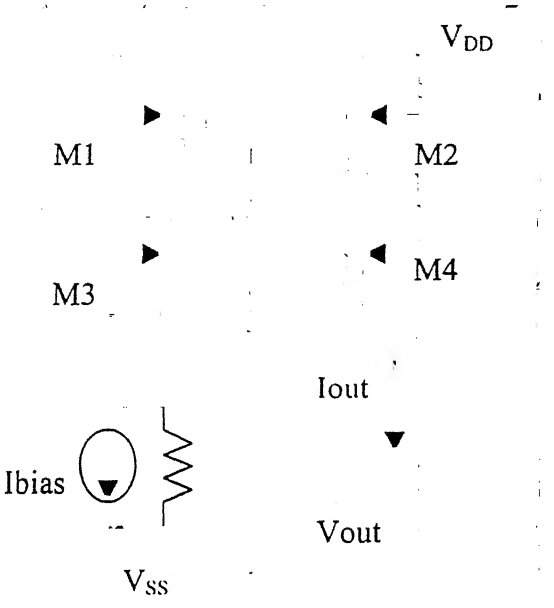

Fig 3.2.2 PMOS Cascode CM

The output impedance (*Roc)* is given by:

$$Roc = ro_2\,(1 + (gm_4 + gmb_4)\,ro_4) + ro_4 \qquad (3.4)$$

where ro_2 and ro_4 are the drain to source resistance of M2 and M4, and gm_4 and gmb_4 are the transconductance and gate-body transconductance of transistor M4.

The minimum output voltage ($Vout_{min}$) is given by:

$$Voc = Vout_{min} = |Vgs_2 + Vgs_4| - |Vt| \qquad (3.5)$$

where Vgs_2 and Vgs_4 are the gate source voltage of M2 and M4 respectively and Vt is the threshold voltage of M4 taking into account the body effect.

The overall active area is given by:

$$AREA = (W1 + W2 + W3 + W4)\, x\, Lmin \qquad (3.6)$$

The above equations can be manipulated to obtain a new set of equations which depicts the specifications of a CCM in terms of it's constraints. They are mentioned below separately for a NMOS CCM and PMOS CCM. For an NMOS CCM the set of equations are :

$$Roc = \frac{1+\lambda n(\Delta V1+Vtno)}{\lambda nIoc}\left[1+\frac{2(1+\lambda n\Delta V2)}{\lambda n(\Delta V1+Vtno)}+\frac{1+\lambda n\Delta V2}{\lambda n\Delta V2}\right]$$

$$Vo_{min} = Vss + 2\Delta V1 + Vtno$$

$$Area = Ld^2\left[\frac{4Id1}{kn'\Delta V1^2(1+\lambda n\Delta V2)}+\frac{4Id1}{kn'\Delta V1^2\{1+\lambda n(\Delta V1+Vtno)\}}\right]$$

For a PMOS CCM the set of equations are:

$$Roc = \frac{1+\lambda p(\Delta V1+|Vtpo|)}{\lambda pIoc}\left[1+\frac{2(1+\lambda p\Delta V2)}{\lambda p(\Delta V1+|Vtpo|)}+\frac{1+\lambda p\Delta V2}{\lambda p\Delta V2}\right]$$

$$Vo_{min} = V_{DD} - 2\Delta V1 - Vtpo$$

$$Area = Ld^2\left[\frac{4Id1}{kp'\Delta V1^2(1+\lambda n\Delta V2)}+\frac{4Id1}{kp'\Delta V1^2\{1+\lambda p(\Delta V1+|Vtpo|)\}}\right]$$

where $\Delta V2$ is the average drain source voltage. i.e $\Delta V2 = |V_{DS}|$

3.2.3 Wilson Current Mirror

The characteristic of a simple basic current mirror (SCM) is improved significantly if negative feedback principle can be applied on it. The Wilson Current Mirror uses this principle to offer stable current values for wide voltage swings and

enhanced output impedance. The schematics of a NMOS Wilson current mirror (WCM) and that of a PMOS WCM are shown in Fig 3.3.1 and Fig 3.3.2 respectively. Assuming M1 and M2 are of the same dimension the mathematical relations are given below:

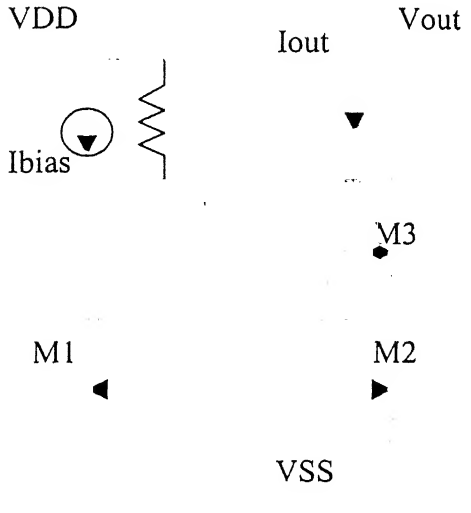

Fig 3.3.1 NMOS Wilson CM

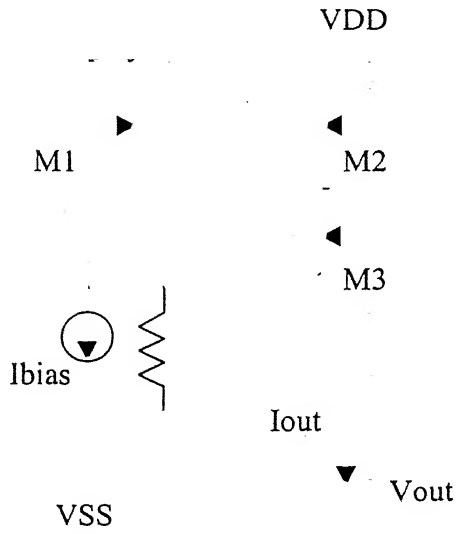

Fig 3.3.2 PMOS Wilson CM

The output impedance (*Row*) is given by:

$$Row = ro_3\{1+gm_2(ro_1 \,||\, ro_2) + \frac{gmb_3}{gm_3} + \frac{1}{ro_3 gm_3}\} \tag{3.7}$$

where ro_1, ro_2 and ro_3 are the drain-source resistances of M1, M2 and M3 and gm_2, gm_3 and gmb_3 are the conductances of M2 and M3 respectively.

The minimum output voltage *(Vow)* is given by:

$$Vow = Vout_{min} = |Vgs_3| + |Vds_4| = |Vgs_3| + |Vgs_4| - |Vt| \tag{3.8}$$

The overall active area is given by:

$$AREA = (W1 + W2 + W3)\, x\, Lmin \tag{3.9}$$

The above equations can be manipulated to obtain a new set of equations which depicts the specifications of a WCM in terms of it's constraints. They are mentioned below separately for a NMOS WCM and PMOS WCM:

For an NMOS WCM the set of equations are :

$$Row = \frac{1+\lambda\, n\Delta V2}{\lambda\, nIow}\left[1+\frac{2(1+\lambda\, n\Delta V2)}{\lambda\, n\Delta V2}+\frac{\lambda\, n\Delta V2}{1+\lambda\, n\Delta V2}\right]$$

$$Vo_{min} = Vss + 2\Delta V1 + Vtno$$

$$Area = Ld^2\left[\frac{4Id1}{kn'\Delta V1^2(1+\lambda\, n\Delta V2)}+\frac{2Id1}{kn'\Delta V1^2[1+\lambda\, n(\Delta V1+Vtn)]}\right]$$

For a PMOS WCM the set of equations are:

$$Row = \frac{1+\lambda\, p\Delta V2}{\lambda\, pIow}\left[1+\frac{2(1+\lambda\, p\Delta V2)}{\lambda\, p\Delta V2}+\frac{\lambda\, p\Delta V2}{1+\lambda\, p\Delta V2}\right]$$

$$Vo_{min} = V_{DD} - 2\Delta V1 - |Vtpo|$$

$$Area = Ld^2\left[\frac{4Id1}{kp'\Delta V1^2(1+\lambda\, p\Delta V2)}+\frac{2Id1}{kp'\Delta V1^2[1+\lambda\, p(\Delta V1+|Vtp|)]}\right]$$

3.3 Voltage Driven Amplifiers

The circuits which will be discussed under this topic are CMOS voltage driven inverting amplifiers. This inverting amplifier, sometimes called an inverter, is one of the primary gain stages of analog amplifiers. The performance of the inverting amplifier can be improved by the use of additional devices. These additional devices appear in cascode configuration and are often termed as cascode amplifiers. The improvements are not only in the area of performance, but also in the area of more degrees of design freedom. The following types of voltage driven amplifiers are been designed and used quite extensively in our work.

1) Simple Voltage Driven CMOS inverters

2) Voltage Driven CMOS inverters with Cascode Load

3) Voltage Driven CMOS Cascode Amplifiers

4) Fully Cascode CMOS Amplifiers

For the design of inverter, the performance objectives are to minimize the total area, to maximize the overall gain of the amplifier, to improve the overall frequency response and also to obtain a good output voltage swing..

Table 3.2 Performance Specification of Voltage Driven Amplifier

Sr No	Symbol	Specification	Typical Objective
1	*Av*	*AC Voltage Gain*	*Maximize*
2.	*fnd*	*Non dominant pole*	*Maximize*
3.	*Area*	*Active Area*	*Minimize*
4.	*Ro*	*Output Impedance*	*Maximize*
5.	Vo_{max}	*Maximum Output Voltage Swing*	*Maximize*
6.	Vo_{min}	*Minimum Output Voltage Swing*	*Minimize*

In our work as we will be using the inverting amplifiers to enhance the overall gain of the Simple 2 stage Miller Compensated op amp. Below given are the detailed explanations of these inverting amplifiers which are used in our work.

3.3.1. Simple Voltage Driven CMOS Inverter

The schematic of a simple voltage driven amplifier is shown in Fig 3.4. It is a current sourcing inverter with an active n-channel load. The mathematical relations which relate the performance specifications to different device characteristics are given below.

The ac voltage gain is given by:

$$Av = \frac{-gm_1}{\frac{1}{ro_1} + \frac{1}{ro_2}} \tag{3.10}$$

where gm_1 is the transconductance of M1 and ro_1 and ro_2 are the drain to source impedances of M1 and M2.respectively.

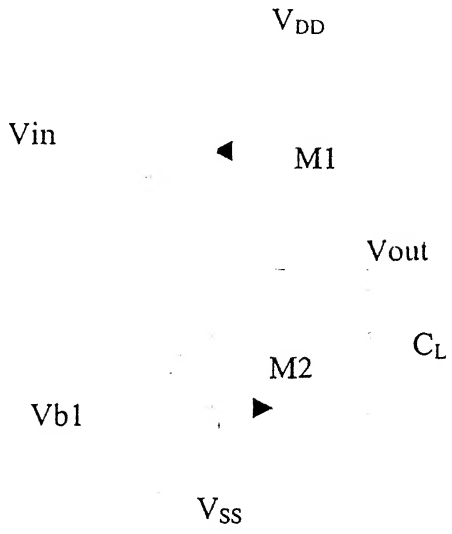

Fig 3.4 Simple Voltage Driven CMOS Inverter

The ac output impedance is given by:

$$Ro = \frac{ro_1 ro_2}{ro_1 + ro_2} \tag{3.11}$$

The overall active area is given by :

$$Area = (W1 + W2)\ x\ Lmin \tag{3.12}$$

The output voltage swing is given by:

$$Vss + \Delta V1 \leq Vo \leq Vin + |Vtpo| \tag{3.13}$$

The above equations can be manipulated to obtain a new set of equations which depicts the specifications of a voltage driven CMOS inverter in terms of it's constraints. They are shown below:

$$Av = \frac{-gm_1}{\frac{1}{ro_1} + \frac{1}{ro_2}}$$

$$fnd = \frac{gm_1}{2\pi C_L}$$

$$Vo_{max} \leq V_{DD} - \Delta V$$

$$Vo_{min} \geq Vss + \Delta V$$

$$Area = Ld^2 \left[\frac{2Id1}{kp'\Delta V1^2\{1+\lambda\, p\Delta V2\}} + \frac{2Id1}{kn'\Delta V1^2\{1+\lambda\, n\Delta V2\}} \right]$$

where *Id1* is the current flowing through the inverting amplifier and $\Delta V1$ is the gate overdrive and $\Delta V2$ is the drain source voltage i. e $|Vds|$ and C_L is the load capacitance.

3.3.2 Voltage Driven CMOS Inverter with Cascode Load

The schematic of a Voltage Driven CMOS inverter with a cascode load is shown in Fig 3.5. A single p-channel transistor serves as the voltage-controlled current source (M1) which is the input device and a cascaded current source (M2 and M3) is the load. It has been assumed that the dimensions of M2 and M3 are same. The effectiveness of this configuration is that the overall ac gain shows a significant rise along with the rise in the overall ac output impedance. The mathematical relations which work well with this topology are given below:

The ac voltage gain is given by:

$$Av = \frac{-gm_1 gm_2}{\frac{1}{ro_2 ro_3} + \frac{gm_2}{ro_1}} \qquad (3.14)$$

where gm_1 and gm_2 are the transconductance of M1 and M2 respectively and ro_1, ro_2 and ro_3 are the drain to source resistance of M1, M2 and M3 respectively.

The ac output impedance is given by:

$$Ro = \frac{gm_2}{\frac{1}{ro_2 ro_3} + \frac{gm_2}{ro_1}} \tag{3.15}$$

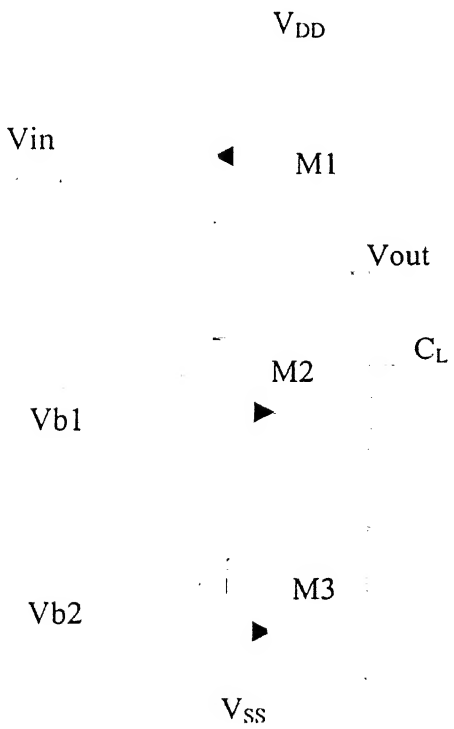

Fig 3.5 CMOS Inverter with Cascode Load

The output voltage swing is given by:

$$Vss + 2\Delta V1 \leq Vo \leq Vin + |Vtpo| \tag{3.16}$$

The overall active area is given by:

$$Area = (W1 + W2 + W3) \times Lmin \tag{3.17}$$

The above equations can be manipulated to obtain a new set of equations which depicts the specifications of a voltage driven CMOS inverter in terms of it's constraints. They are shown below:

$$Av = \frac{-gm_1 gm_2}{\frac{1}{ro_2 ro_3} + \frac{gm_2}{ro_1}}$$

$$fnd = \frac{gm_1}{2\pi C_L}$$

$$Vo_{max} \leq V_{DD} - \Delta V$$

$$Vo_{min} \geq Vss + 2\Delta V$$

$$Area = Ld^2 \left[\frac{2Id1}{kp'\Delta V1^2\{1+\lambda\, p\Delta V2\}} + \frac{4Id1}{kn'\Delta V1^2\{1+\lambda\, n\Delta V2\}} \right]$$

3.3.3 Voltage Driven CMOS Cascode Amplifier

The schematics of Voltage Driven Cascode amplifier is given on Fig 3.6. The Cascode amplifiers are used to improve the overall frequency response of the inverters. These type of amplifiers offer an isolation between the input terminals and the output terminal and as a result of which the Miller's effect is negligible. The overall gain of the amplifier shows an improvement. The influence of the cascode transistor is felt on the impedance seen by the drain of the input device which reduces drastically. The mathematical relations which holds well for this topology of inverter are given below:

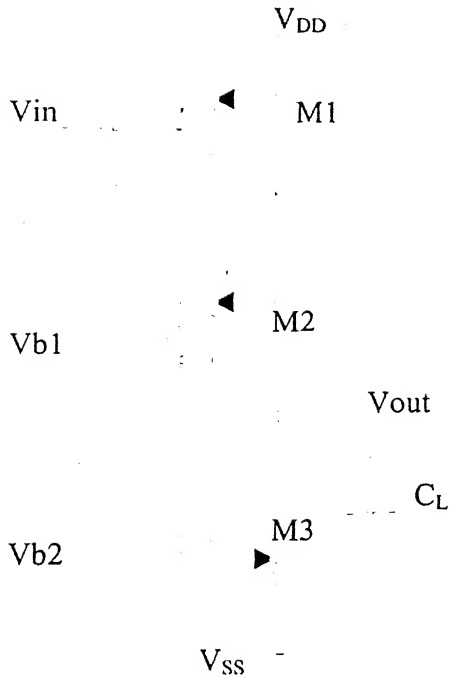

Fig 3.6 CMOS Cascode Amplifier

The ac gain is given by:

$$Av = \frac{-gm_1 gm_2}{\frac{1}{ro_2 ro_1} + \frac{gm_2}{ro_3}} \tag{3.18}$$

where gm_1 and gm_2 are the transconductance of M1 and M2 respectively and ro_1, ro_2 and ro_3 are the drain to source resistances of M1, M2 and M3 respectively.

The ac output impedance is given by:

$$Ro = \frac{gm_2}{\frac{1}{ro_2 ro_1} + \frac{gm_2}{ro_3}} \tag{3.19}$$

The output voltage swing is given by:

$$Vss + \Delta V1 \leq Vo \leq Vin + |Vtpo| - \Delta V1 \tag{3.20}$$

The overall active area is given by:

$$Area = (W1 + W2 + W3) \times Lmin \tag{3.21}$$

The above equations can be manipulated to obtain a new set of equations which depicts the specifications of a voltage driven CMOS inverter in terms of it's constraints. They are shown below:

$$Av = \frac{-gm_1 gm_2}{\frac{1}{ro_2 ro_1} + \frac{gm_2}{ro_3}}$$

$$fnd = \frac{gm_1}{2\pi C_L}$$

$$Vo_{max} \leq V_{DD} - 2\Delta V$$

$$Vo_{min} \geq Vss + \Delta V$$

$$Area = Ld^2 \left[\frac{2Id1}{kp'\Delta V1^2\{1 + \lambda p\Delta V2\}} + \frac{2Id1}{kn'\Delta V1^2\{1 + \lambda n\Delta V2\}} + \frac{2Id1}{kp'\Delta V1^2} \right]$$

3.3.4 Fully Cascode CMOS Amplifier

The schematics of a Voltage Driven Fully Cascode Amplifier is given in Fig. 3.7. The addition of a fourth transistor to the voltage driven Cascode amplifier to achieve the cascode CMOS inverter is probably the best method of significantly increasing the ac gain of the inverter. The effect of the fourth transistor is to cascode the active current source load and to boost the output resistance seen by input device M1 and the cascode transistor M2. This causes the output impedance of the inverter to increase the gain. The mathematical relations which holds true for this topology are given below:

The ac gain is given by:

$$Av = \frac{-gm_1 gm_2 gm_3}{\frac{gm_2}{ro_3 ro_4} + \frac{gm_3}{ro_1 ro_2}} \tag{3.22}$$

The ac output impedance is given by:

$$Ro = \frac{gm_2 gm_3}{\frac{gm_2}{ro_1 ro_4} + \frac{gm_3}{ro_1 ro_2}} \quad (3.23)$$

The output voltage swing is given by:

$$Vss + 2\Delta V1 \leq Vo \leq Vin + |Vtpo| - \Delta V1 \quad (3.24)$$

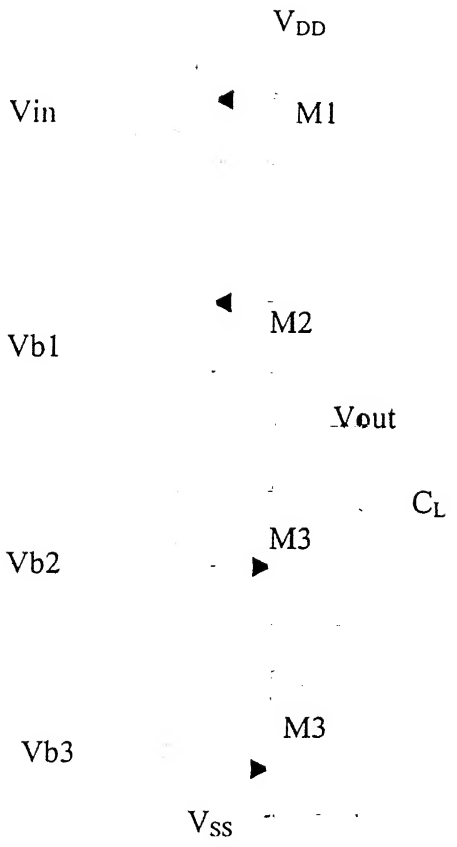

Fig 3.7 Fully Cascode CMOS Amplifier

The overall active area is given by:

$$Area = (W1 + W2 + W3 + W4) \times Lmin \quad (3.25)$$

The above equations can be manipulated to obtain a set of equations which depicts the specifications of a fully Cascode inverting amplifier in terms of it's constraints. They are shown below:

$$Av = \frac{-gm_1 gm_2 gm_3}{\frac{gm_2}{ro_3 ro_4} + \frac{gm_3}{ro_1 ro_2}}$$

$$fnd = \frac{gm_1}{2\pi C_L}$$

$$Vo_{max} \leq V_{DD} - 2\Delta V$$

$$Vo_{min} \geq Vss + 2\Delta V$$

$$Area = Ld^2 \left[\frac{2Id1}{kp'\Delta V1^2\{1+\lambda\, p\Delta V2\}} + \frac{2Id1}{kn'\Delta V1^2\{1+\lambda\, n\Delta V2\}} + \frac{2Id1}{kp'\Delta V1^2} + \frac{2Id1}{kn'\Delta V1^2} \right]$$

3.4 Differential Amplifiers

The differential amplifier has become a very useful circuit because of its ability to amplify differential signals. Any two signal can be decomposed into a difference mode signal and a common mode signal. The differential amplifier is characterized by its differential mode gain and its common mode gain. The ratio is called the common mode rejection ratio (CMRR) which should be ideally as large as possible. The following types of differential amplifiers are being used quite extensively in our work.

1) CMOS Differential pair with a Current Mirror Load
2) Cascode CMOS Differential pair with a Current Mirror Load

For the design of differential pairs, the performance objectives are to minimize the total area, to maximize the overall gain of the differential amplifier, to improve the overall frequency response and also have a high CMRR.

Table 3.3 Performance specifications of Differential Pair

Sr No	Symbol	Specification	Typical Objective
1.	*Av*	*Gain*	*Maximize*
2.	*CMRR*	*Common Mode Rejection Ratio*	*Maximize*
3.	*UGF*	*Unity Gain Frequency*	*Maximize*
4.	*Area*	*Overall active area*	*Minimize*

In our work as we will be using the differential pairs in the input stage of the Simple 2 stage Miller Compensated op amp. Below given are the detailed explanations of these differential pairs which are used in the input stage of a Simple 2 stage Miller Compensated op amp.

3.4.1 CMOS Differential Pair with a Current Mirror Load

Given below in Fig 3.8 is a simple differential pair with a current mirror load. In this topology the advantage is that the differential output signal is converted to single ended output signal without any extra components required. In this circuit the output voltage or current is taken from the drains of M2 and M4. It has been assumed that the dimensions of M1 and M2 are equal and also dimensions of M3 and M4 are same. The operation of this circuit is as follows. If a differential voltage, V_{ID}, is applied between the gates then half is applied to the gate source of M1 and half to the gate source of M2. The result is to increase I_{D1} and decrease I_{D2} by equal increments, ΔI. The ΔI change is then mirrored into the current mirrors. The mathematical relations which works well for this topology are given below:

The differential mode gain is given by:

$$Adm = \frac{gm_1}{gd_2 + gd_4} \tag{3.26}$$

where gm_1 is the conductance of M1 and gd_2 and gd_4 are the drain conductance of M2 and M4 respectively.

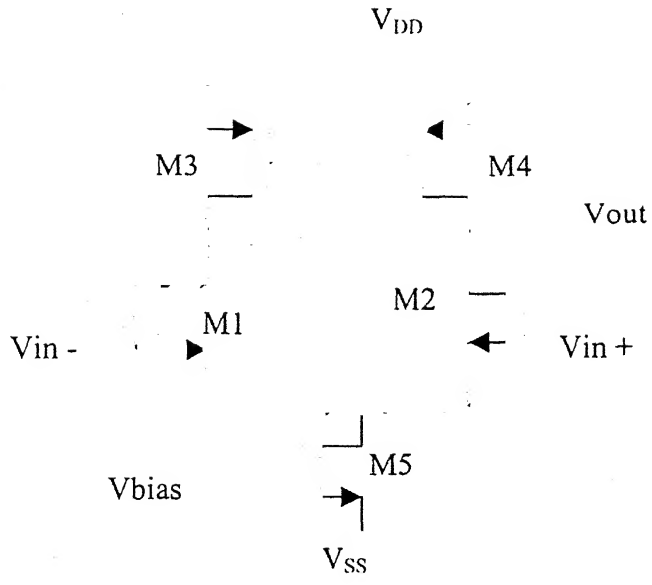

Fig :3.8 CMOS Differential pair with CM load

The common mode gain is given by:

$$Acm = \frac{gd_5 gd_1}{2gm_4(gd_4 + gd_1)} \tag{3.27}$$

where gd_5, gd_1 and gd_4 are the drain conductance of M5, M1 and M4 respectively and gm4 is the conductance of M4.

$$CMRR = \frac{2gm_1 gm_4}{gd_5 gd_1} \tag{3.28}$$

The output impedance is given by :

$$Ro = \frac{1}{gd_2 + gd_4} \tag{3.29}$$

The unity gain frequency is given by:

$$UGF = \frac{gm_1}{2\pi\, Cc} \tag{3.30}$$

where Cc is the compensation capacitance.

The overall active area is given by:

$$AREA = (W1 + W2 + W3 + W4) \times Lmin \quad (3.31)$$

The above equations can be manipulated to obtain a set of equations which depicts the specifications of a fully simple CMOS differential amplifier in terms of it's constraints. They are shown below:

$$Av = \frac{gm_1}{gd_2 + gd_4}$$

$$CMRR = \frac{2gm_1gm_4}{gd_5gd_1}$$

$$UGF = \frac{gm_1}{2\pi\, Cc}$$

$$Area = Ld^2 \left[\frac{4Id1}{kp'\Delta V1^2\{1 + \lambda\, p\Delta V2\}} + \frac{4Id1}{kn'\Delta V1^2\{1 + \lambda\, n\Delta V2\}} \right]$$

3.4.2 Cascode CMOS differential pair with a current mirror load

The simple CMOS differential pair suffer from a low power supply rejection ratio (PSSR). The PSSR can be increased by minimizing the stray capacitance. Parasitic capacitances inside the op amp also contribute to the power supply noise gain. Different steps are taken to reduce the noise gain which leads to increase in thermally generated noise and also increase in the chip area. A technique which eliminates this problem, at the cost of slightly reduced common-mode input range, is to use a cascode circuitry in the input stage. The added device then M5 and M6 then buffer the drains of M1 and M2 from the variations of V_{DD} provided Vbias is independent of the supply voltage. It has been assumed that the dimensions of M1 and M2, the dimensions of M3 and M4 and also dimensions of M5 and M6 are same. The schematic for such a topology is shown in Fig: 3.9 and the detailed mathematical expressions are mentioned below.

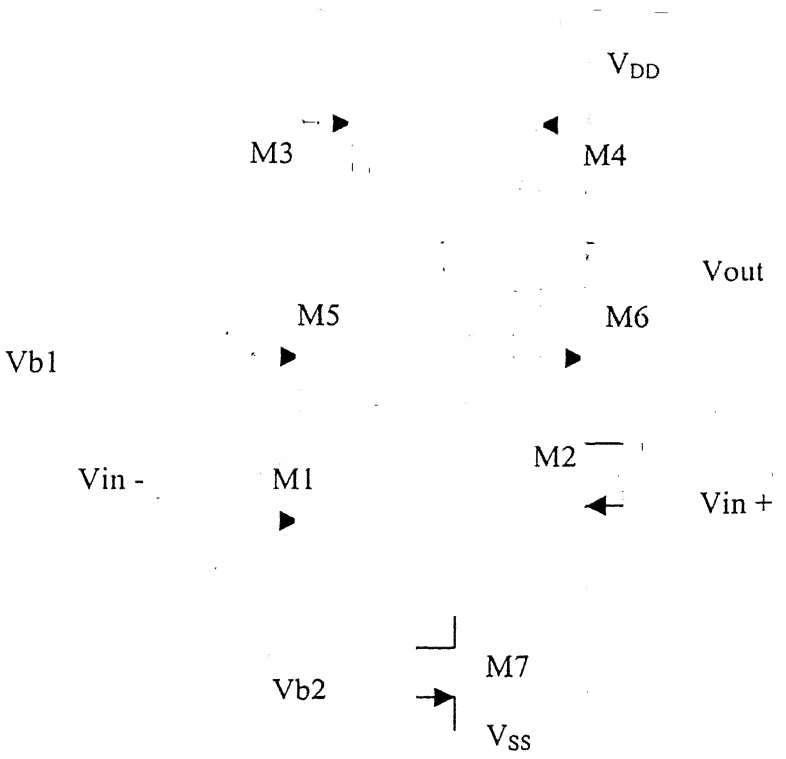

Fig 3.9 Cascode CMOS differential pair with CM load

The differential mode gain is given by:

$$Adm = \frac{gm_1 gm_6}{gd_2 gd_6 + gd_4 gm_6} \tag{3.32}$$

The common mode gain is given by:

$$Acm = \frac{gm_6 gd_7 gd_4 gd_6 gd_2}{2gm_1(gd_6 gd_2 + gm_6 gd_4)^2} \tag{3.33}$$

The CMRR is given by:

$$CMRR = \frac{2gm_1^2(gd_6 gd_2 + gm_6 gd_4)}{gd_4 gd_6 gd_2} \tag{3.34}$$

The UGF is given by:

$$UGF = \frac{gm_1}{2\pi\, Cc} \tag{3.35}$$

The output impedance is given by:

$$Ro = \frac{gm_6}{gd_6 gd_2 + gm_6 gd_4} \tag{3.36}$$

The overall active area is given by:

$$AREA = (W1 + W2 + W3 + W4 + W5 + W6) \, x \, Lmin \tag{3.37}$$

The above equations can be manipulated to obtain a set of equations which depicts the specifications of a fully simple CMOS differential amplifier in terms of it's constraints. They are shown below:

$$Av = \frac{gm_1 gm_6}{gd_2 gd_6 + gd_4 gm_6}$$

$$CMRR = \frac{2gm1^2 (gd_6 gd_2 + gm_6 gd_4)}{gd_4 gd_6 gd_2}$$

$$UGF = \frac{gm_1}{2\pi \, Cc}$$

$$Area = Ld^2 \left[\frac{4Id1}{kp' \Delta V1^2 \{1 + \lambda \, p\Delta V2\}} + \frac{4Id1}{kn' \Delta V1^2 \{1 + \lambda \, n\Delta V2\}} + \frac{4Id1}{kn' \Delta V1^2} \right]$$

CHAPTER 4
IMPLEMENTATION

4.1 Introduction

In this chapter we look into the details of how topology generation of 2 stage Miller compensated op amp is done as discussed briefly earlier in chapter 2. The validity of our topology generation work is discussed in detail here. At the top most level design of a 2 stage Miller compensated op amp we don't have any details of the transistors level design of this op amp. The op amp appears as affixed connection of building blocks such as load current mirrors, differential pairs, bias current mirrors and trans conductance amplifiers. Translation of the input performance specifications is then carried out using GA and finally we obtain the optimized set of specs for each sub block.

4.2 Representation of sub blocks

The current mirror, also referred to as current source/sink is represented as a two terminal element whose current is constant for any voltage across the source. A DC voltage source is used to bias the implementation of the current sources or sinks. It is also seen that there is a minimum voltage Vo_{min} below which the current source will not be a good approximation to Io. Further it is seen that even in the region where the current source/sink is a reasonably good approximation to Io, the actual source/sink deviates a due to resistance Ro which represents the parallel resistance of the current source/sink and ideally is infinite. Thus the three major aspects by which a current source/sink is characterized are Vo_{min} and Ro (R_{cm} & R_{bias}) along with Io. In this work we represent the Current Mirror of the active load stage by a current source and a Current Mirror of the biasing stage by a current sink. These have shown schematically in Fig 4.2.1 and Fig 4.2.2 given below:

The trans conductance amplifier used in this work is a voltage driven inverting amplifier. In its most simple form, the inverting amplifier can be represented by two

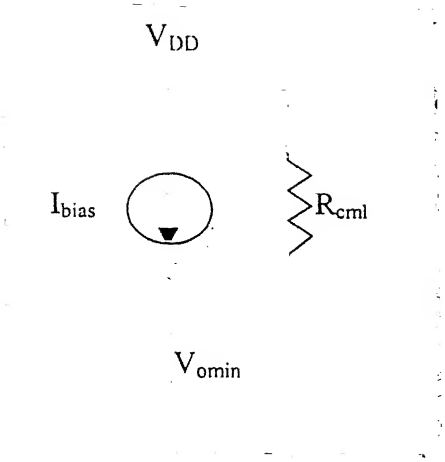

Fig 4.2.1 Schematic representation of a Current Mirror load

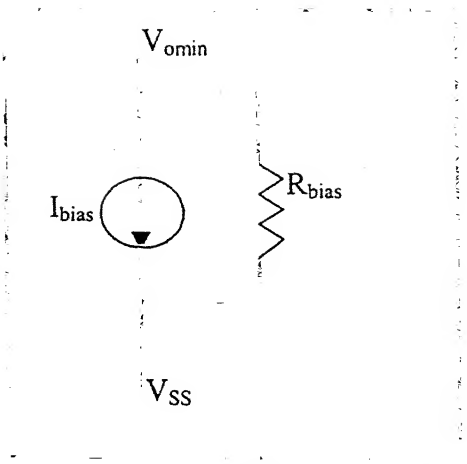

Fig 4.2.2 Schematic representation of a Current Mirror Bias

blocks. One of the blocks is a voltage controlled current source and the other is a load. In this case, the current is controlled by the voltage at the input terminal. The voltage-controlled current source is combined with the two terminal load results a sourcing inverter. It is called a sourcing inverter because it sources the current in the load. The major aspects by which a sourcing inverter is characterized are the impedances of the load (Rol), the trans conductance gain (gmg) of the voltage controlled current source and it's output impedance (Rog). This has been shown schematically in Fig 4.2.3 given below.

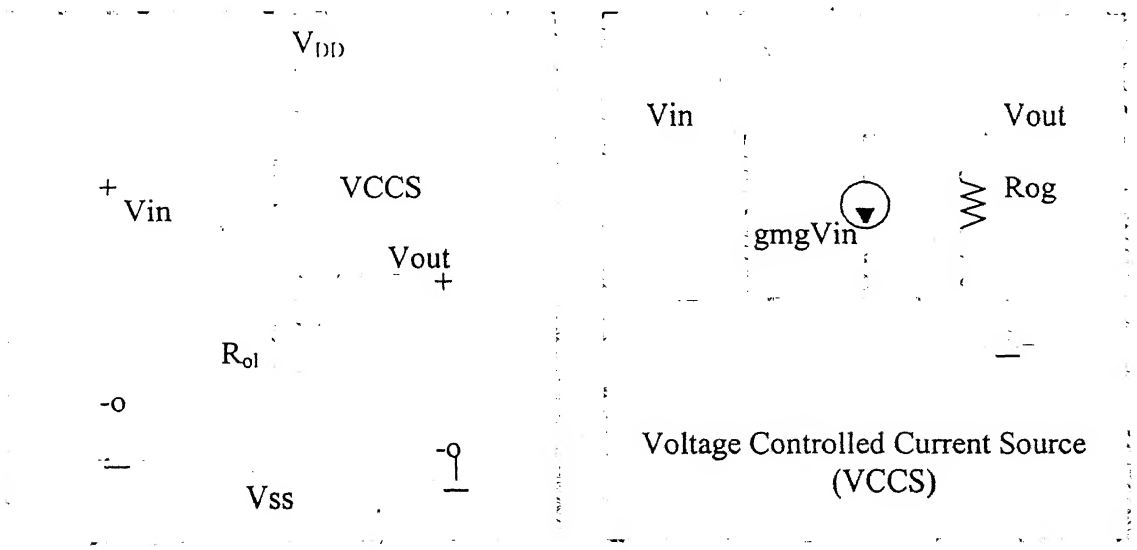

Fig 4.2.3 Schematic representation of a Transconductance Amplifier

The differential amplifier has become a very useful circuit because of it's ability to amplify differential signals. The differential amplifier is characterized by its differential gain and its common mode gain. In our work we have represented a differential amplifier as a Voltage controlled current source amplifier with an active load. The parameters which have been used to represent a differential amplifier are the output impedances of the current mirrors which act as the active load (Rcml), the trans conductance gain (gmi) of the amplifier and it's output impedance (Rdp). This has been shown schematically in Fig 4.2.4

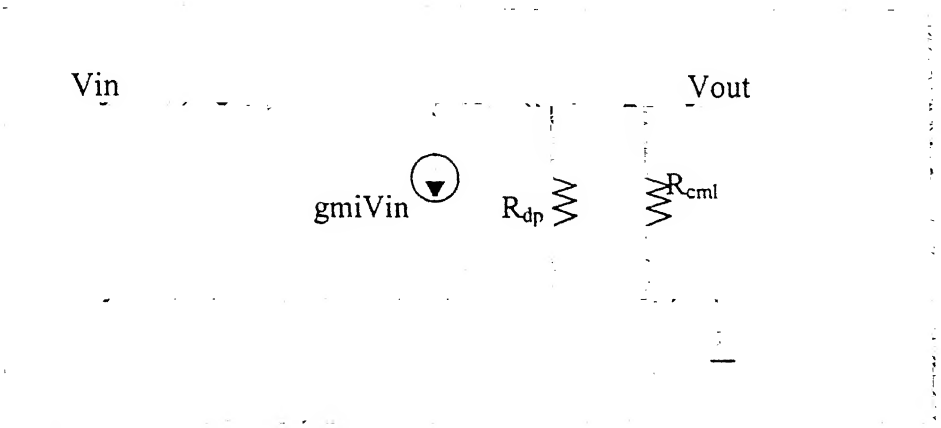

Fig 4.2.4 Schematic representation of a Differential Amplifier

4.3 Two Stage Miller Compensated Operational Amplifier

Operational amplifier (op amp) is a basic building block used in wide variety of analog circuits, e. g A/D converters, switched capacitor filters, etc. Therefore the overall topology generation and design of op amp is of tremendous importance in order to meet performance specifications for circuits of larger complexity. Before we can invoke the translation process to refine op amp specifications into the current mirrors, differential pair etc an op amp style has to be selected. Selection happens at all levels of the hierarchy. For example, mirrors, differential pairs, and trans-conductance amplifiers all come in various styles as well, although now the sub-blocks in each of these styles are actually transistors. In the present work we have implemented only the 2 - stage Miller compensated op amp for detailed analysis. A schematic of 2 stage Miller Compensated

op amp is shown in Fig 4.3. The performance specifications for which the program is written are tabulated in the table 4.1. given below:

Table 4.1 Performance specifications of a 2 stage Miller Compensated op amp

S.r No	Symbol	Performance Specifications	Typical Objective
1.	*Av*	*Overall Voltage Gain*	*Maximize*
2.	*CMRR*	*Common Mode Rejection Ratio*	*Maximize*
3.	*PM*	*Phase Margin*	*User Specified*
4.	*UGF*	*Unity Gain Frequency*	*Maximize*
5.	*SR*	*Slew Rate*	*User Specified*
6.	*PD*	*Power Dissipation*	*User Specified*
7.	*Area*	*Overall Active Area*	*Minimize*
8.	Vo_{min}	*Minimum Output Voltage*	*User Specified*
9.	Vo_{max}	*Maximum Output Voltage*	*User Specified*
10.	C_L	*Output Load Capacitance*	*User Specified*
11.	*Cc*	*Compensating Capacitance*	*Assumed.*

Initially, a particular topology to be designed is selected at the top most level of the hierarchy. This is followed by a design phase where the input specifications are translated from the top most level in the hierarchy to the next lower, more concrete level. Genetic Algorithm based optimization is used during this translation process to obtain the new optimized set of specifications for each of the building sub blocks. The set of analytical equations which have been widely used in the translation process are given below:

$$Av = \frac{gmigmgRcmlRdpRogRol}{(Rdp + Rcml)(Rog + Rol)} \tag{4.1}$$

$$CMRR = \frac{2gmi^2 Rbias^2 (Rcml + Rdp)}{(Rdp + Rbias)} \tag{4.2}$$

$$UGF = \frac{gmi}{2\pi\, Cc} \tag{4.3}$$

$$fnd = \frac{gmg}{2\pi\, Cl} \tag{4.4}$$

$$PM = 90^{0} - \tan^{-1}\frac{UGF}{fnd} \tag{4.5}$$

$$Pd = (Ibias + I_{D5} + 2I_{D1})(V_{DD} - Vss) \tag{4.6}$$

$$Area = \Sigma WixLi \tag{4.7}$$

$$SR = \frac{Ibias}{Cc} = \frac{I_{D5}}{Cl} \tag{4.8}$$

$$Vo_{min} \geq Vss + k\Delta V \tag{4.9}$$

$$Vo_{max} \leq V_{DD} - k\Delta V \tag{4.10}$$

where Rcml, Rbias are the output impedances of the load and bias stage current mirrors. Rdp, Rog are the impedances looking into the drain of the input stage transistors of differential pair and the trans conductance amplifiers. Rol is the load impedance of the trans conductance amplifier. gmi and gmg are the trans conductance of the input transistor of the differential pair and the trans conductance amplifier. Cc and Cl are the compensation capacitance and the output load capacitance respectively, k is either 1 or 2 depending upon whether the gain and the load stage is simple or cascode. Ibias, I_{D5}, and I_{D1} are the biasing current, current flowing through the trans conductance amplifier and the current flowing through the differential pair respectively. Wi and Li are the width and the length of the ith transistor.

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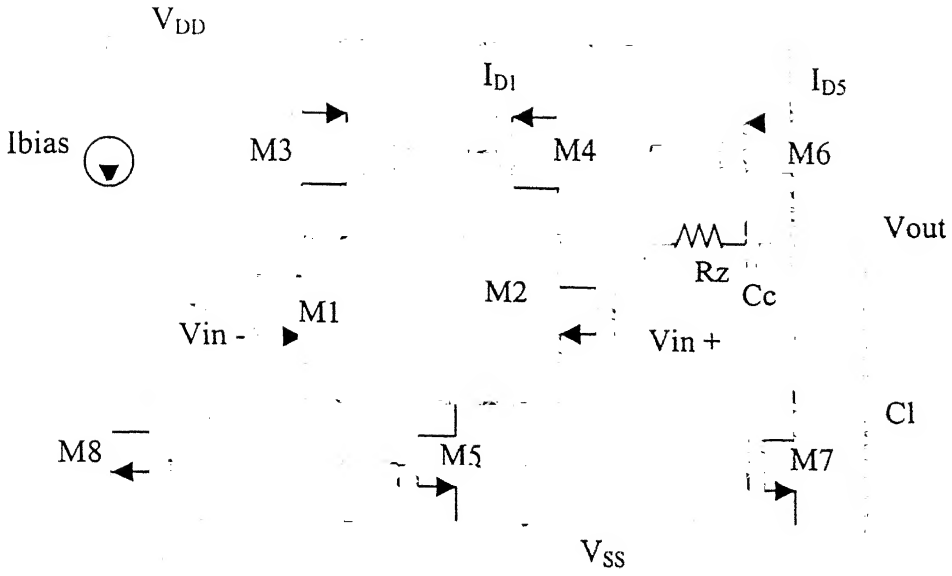

Fig 4.3 A 2 stage Miller Compensated Op amp.

4.4 Topology Selection Procedure

The set of optimized specifications for the sub blocks which are obtained after the translation of the input performance specifications at the top most level of the hierarchy are $Rcml_{sp}$, $Rbias_{sp}$, Rdp_{sp}, Rog_{sp}, Rol_{sp}, gmi_{sp}, gmg_{sp}. The specifications obtained for each sub block are divided into two sets S_0 and S_1. One subset of the specs (S_0) along with the choice of a topology is used to generate a new value for the other subset S_1'. Depending on the match between the elements of S_1 and S_1' the topology is considered a success or a failure. The following constraints given in Table 3.5-3.8 should be satisfied before selecting a particular topology of each possible sub block:

- Current Mirror Load

Table 3.5 Topology selection criteria of a Current Mirror Load

Sr No	Constraints	Implications
1.	$Rcml_{scm} \geq Rcml_{sp,}$ $Vo < V_{DD} - 2\Delta V - Vt$	*Select the SCM, CCM and WCM*

2.	$Rcml_{ccm} \geq Rcml_{sp}$ $Vo<V_{DD}-2\Delta V-Vt$	*Select the CCM and WCM*
3.	$Rcml_{wcm} \geq Rcml_{sp}$ $Vo<V_{DD}-2\Delta V-Vt$	*Select the only possible WCM.*
4.	$Rcml_{scm} \geq Rcml_{sp,}$ $V_{DD}-2\Delta V-Vt<V<V_{DD}-\Delta V$	*Select the only possible SCM*

- Current Mirror Bias

Table 3.6 Topology selection criteria of a Current Mirror Bias

Sr No	Constraints	Implications
1.	$Rbias_{scm} \geq Rbias_{sp}$	*Select the SCM, CCM and WCM*
2.	$Rbias_{ccm} \geq Rbias_{sp}$	*Select the CCM and WCM*
3.	$Rbias_{wcm} \geq Rbias_{sp}$	*Select the only possible WCM.*

- Differential Pair

Table 3.7 Topology selection criteria of a Differential Pair

Sr No	Constraints	Implications
1.	$gmi \geq gmi_{sp}$, $Rdp_{sim} \geq Rdp_{sp}$	*Select the SDP and CDP*
2.	$gmi \geq gmi_{sp,}$ $Rdp_{cas} \geq Rdp_{sp}$	*Select the only possible CDP*

- Trans Conductance Amplifier

Table 3.8 Topology selection criteria of a Trans Conductance Amplifier

Sr No	Constraints	Implications
1.	$gmg \geq gmg_{sp,}$ $Rog_{sim} \geq Rog_{sp,}$ $Vomax < V_{DD} - \Delta V$	*Select the Simple and Cascode Gain stage*
2.	$gmg \geq gmg_{sp,}$ $Rog_{cas} \geq Rog_{sp,}$ $Vomax < VDD - 2\Delta V$	*Select the only possible Cascode Gain stage*

3. $gmg \geq gmg_{sp}$, $Rol_{sim} \geq Rol_{sp}$, *Select the Simple and Cascode Load stage*
$Vo_{min} > Vss + \Delta V$

4. $gmg \geq gmg_{sp}$, $Rol_{cas} \geq Rol_{sp}$, *Select the only possible Cascode Load stage.*
$Vomin > Vss + 2\Delta V$

where $Rcml_{scm}$, $Rcml_{ccm}$, $Rcml_{wcm}$ are the output impedances of the SCM, CCM and WCM load current mirror and $Rbias_{scm}$, $Rbias_{ccm}$, $Rbais_{wcm}$ are the output impedances of the SCM, CCM and WCM bias current mirror. gmi and gmg are the trans conductance of the input transistor of the differential pair and the trans conductance amplifier. Rdp_{sim} and Rdp_{cas} are the impedances looking into the drain of the input stages of SDP and CDP. Rol_{sim}, Rol_{cas} are the impedances of the simple load and cascode load stage, Rog_{sim}, Rog_{cas} are the impedances of the simple and cascode gain stage of the transconductance amplifier. All the above mentioned parameters are obtained by using the relations which relate the parameters to the device characteristics.

Final topology is selected from among the successful topologies using a suitable figure of merit. This can be found out by a set of functions which has been defined for each sub block which are mentioned below. Our goal is to select the topology which gives the minimum function value. The minimizing functions for the possible building sub blocks are:

- Current Mirror Load

$$\min(f) = w1\frac{Area_{cm} - Area_{scm}}{Area_{scm}} + w2\frac{Av_{sp} - Av_{ob}}{Av_{sp}} + w3\frac{CMRR_{sp} - CMRR_{ob}}{CMRR_{sp}}$$

- Current Mirror Bias

$$\min(f) = w1\frac{Area_{cm} - Area_{scm}}{Area_{scm}} + w2\frac{CMRRs_{p} - CMRR_{ob}}{CMRR_{sp}}$$

- Differential Pair

$$\min(f) = w1\frac{Area_{dp} - Area_{sdp}}{Area_{sdp}} + w2\frac{Av_{sp} - Av_{ob}}{Av_{sp}} + w3\frac{CMRR_{sp} - CMRR_{ob}}{CMRR_{sp}} + 4w4\frac{gmi_{sp} - gmi_{ob}}{gmi_{sp}}$$

- Trans Conductance Amplifier

$$\min(f) = w1\frac{Area_{gs} - Area_{sgsl}}{Area_{sgsl}} + w2\frac{Av_{sp} - Av_{ob}}{Av_{sp}} + w3\frac{Av_{sp} - Av_{ob}}{Av_{sp}} + 2w4\frac{gmg_{sp} - gmg_{ob}}{gmg_{sp}}$$

$Area_{cm}$ is the active area of a current mirror, $Area_{scm}$ is the active area of a SCM. $CMRR_{sp}$ and Av_{sp}, are the specified Common Mode Ratio and Gain respectively of the op amp which are obtained using the parameters which are the specifications of the sub blocks, obtained during the translation phase. gmi_{sp} and gmg_{sp} are the trans conductance of the input differential stage and the trans conductance amplifier respectively which are the specifications of the sub blocks obtained during the translation phase. $CMRR_{ob}$ and Av_{ob} are the values of CMRR and Av of the op amp obtained using the analytical relations which are in terms of device characteristics. gmi_{ob} and gmg_{ob} are the values of trans conductance of the differential pair and the trans conductance amplifier which are obtained using the analytical relations which are in terms of device characteristics. w1, w2, w3 and w4 are the weights attached ($\sum wi = 1$).

4.5 Implementation Results

In our work we have assumed the values of Cc to be 5pf and also at the same time taken into consideration that the value of C_L which have been specified to the user as 1 pf. In each of the experiments shown below we are first given a set of input performance specifications which are shown in tabular form. After the translation process we obtain the new set of optimized specifications which have been shown in tabular form just below the input specifications table. Using this set of new sub block specifications back calculation is done to obtain the input performance specifications again shown in table just below the sub block specifications table. Then finally topology selection is done for the Current Mirror Load, Current Mirror Bias and the Differential Pair sub blocks which are shown serially in a tabular form.

Experiment 1

Input Specs	Av	CMRR	SR (V/μs)	Pd (mw)	UGF (MHz)	PM (degree)	Vomax (V)	Vomin (V)
Values	9000	$25x10^4$	5	0.4	1	65^0	4.41	-4.41

After translation of input specifications using GA into constraints for the sub blocks::

Specs	Rcml (MΩ)	Rbias (MΩ)	Rdp (MΩ)	Rog (MΩ)	Rol (MΩ)	gmi (μmho)	gmg (μmho)
Values Obtained	52.387	4.096	4.3096	7.483	17.126	34	13

Specs	Av	CMRR	UGF (MHz)
Values obtained	9166.5664	261708.328	1.080394

Topology selection:

- Current Mirror Load

Specifications	Rcml (MΩ)	I_{D1} (μA)	Vomin (Volts)
Value specified	52.3872672	5	3.66
Topologies Available	SCM	CCM	WCM
Rcml obtained (MΩ)	86.956	353.7597	529.447
Topologies Possible	Yes	X	X
Function value	-0.08011	—	—
Topology Selected	Simple Current Mirror (SCM)		

Device Parameters	$(W/L)_1$	$(W/L)_2$	Area (μm^2)
Values Obtained	11.5704/3	11.5704/3	69.443
Parameters	Rcml (MΩ)	I_{D1} (μA)	Vout (V)
SPICE Results	105.5657	4.819	3.219

- Current Mirror Bias

Specifications	Rbias (MΩ)	I_{D1} (μA)	Vomin (Volts)
Value specified	4.096	5	2.15
Topologies Available	SCM	CCM	WCM

Rbias obtained (MΩ)	19.047	109.39681	167.303616
Topologies Possible	Yes	Yes	Yes
Function value	-3.390071	-25.3808	-40.1079
Topology Selected	Wilson Current Mirror (WCM)		
Device Parameters	$(W/L)_1 = (W/L)_2$	$(W/L)_3$	Area (μm^2)
Values Obtained	11.574/3	11.0585/3	102.62
Parameters	Rbias (MΩ)	I_{D1} (μA)	Vout (V)
SPICE Results	197.28191	4.7161	-1.23

- Differential Pair

Specifications	gmi (μmhos)	Rdp (MΩ)	Id1 (μA)
Values	34	4.3096	5
Topologies available	SDP	CDP	
gmi obtained (μmhos)	56	56	
Rdp obtained (MΩ)	4.7619	62.988	
Topologies possible	Yes	Yes	
Function value	-0.6471	-2.121	
Final topology selected	Cascode Differential Pair (CDP)		
Device Parameters	$(W/L)_1 = (W/L)_2$	$(W/L)_3=(W/L)_4$	Area (μm^2)
Values Obtained	11.547/3	11.0856/3	135.795
Parameters	gmi (μmhos)	I_{D1} (μA)	Rdp (MΩ)
SPICE Results	45.718	4.231	14.819

- Trans Conductance Amplifier

Specifications	gmg (μmhos)	Rog (MΩ)	Rol (MΩ)	Id5 (μA)	Vomax (V)	Vomin (V)
Values	13	7.483	17.126	5	4.41	-4.41
Topologies available	SGSL	SGCL		CGSL	CGCL	

gmg (μmhos)	obtained	28	28	28	28
Rog (MΩ)	obtained	86.956	86.956	262.549	262.549
Rol (MΩ)	obtained	190.476	314.940	190.476	314.940
Topologies possible		Yes	Yes	X	X
Function value		-2.20174	-1.2315		
Final Topology selcted		Simple Gain Simple Load stage (SGSL)			

Parameters	$(W/L)_1$	$(W/L)_3$	Area (μm^2)
Values	5.787/3	11.57407/3	52.08331

Parameters	gmg (μmhos)	Rog (MΩ)	Rol (MΩ)	Id5 (μA)	Vomin	Vomax
SPICE results	25.81	142.51	235.891	4.178	4.12	-4.12

- Overall spice simulation results

Variables	Av	CMRR	UGF (MHz)	PM (degree)	Vomax	Vomin
Spice results	1700	$16x10^3$	0.75	43.4^0	4.12	-4.22

The final topology of the designed 2 stage Miller Compensated op amp is made up of the following building sub blocks:

Simple Current Mirror Load

Wilson Current Mirror Bias

Cascode Differential Pair

Transconductance amplifier with Simple gain and Simple load stage.

It is shown in Fig: 4.4

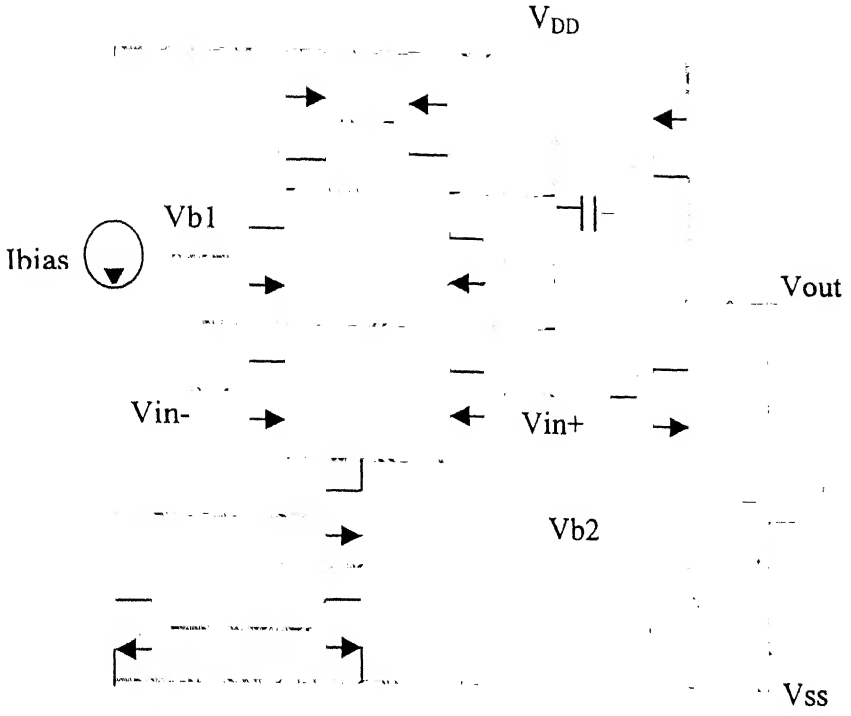

Fig 4.4 Topology generated from Experiment 1

Experiment 2

Input Specs	Av	CMRR	SR (V/μs)	Pd (mw)	UGF (MHz)	PM (degree)	Vomax (V)	Vomin (V)
Values	$4X10^4$	$42.5X10^4$	20	1.5	2.5	75^0	4.0	-4.0

After translation of input specifications using GA into constraints for the sub blocks::

Specs	Rcml (MΩ)	Rbias (MΩ)	Rdp (MΩ)	Rog (MΩ)	Rol (MΩ)	gmi (μmho)	gmg (μmho)
Values Obtained	15.225	4.2903	9.2645	1.5806	39.648	80	59

Specs	Av	CMRR	UGF (MHz)
Values obtained	41324.457	425686.593	2.5421

Topology selection:

- Current Mirror Load

Specifications	Rcml (MΩ)	I_{D1} (μA)	Vomin (Volts)
Value specified	15.225	15	3.65
Topologies Available	SCM	CCM	WCM
Rcml obtained (MΩ)	28.9855	117.919	176.482
Topologies Possible	Yes	X	X
Function value	-0.097591	—	—
Topology Selected	Simple Current Mirror (SCM)		
Device Parameters	$(W/L)_1$	$(W/L)_2$	Area (μm^2)
Values Obtained	43.722/3	34.722/3	208.333
Parameters	Rcml (MΩ)	I_{D1} (μA)	Vout (V)
SPICE Results	92.718	13.156	3.517

- Current Mirror Bias

Specifications	Rbias (MΩ)	I_{D1} (μA)	Vomin (Volts)
Value specified	4.2903	15	2.15
Topologies Available	SCM	CCM	WCM
Rbias obtained (MΩ)	6.3492	36.46561	55.76787
Topologies Possible	Yes	Yes	Yes
Function value	-0.450642	-9.7288	-16.86965
Topology Selected	Wilson Current Mirror (WCM)		
Device Parameters	$(W/L)_1 = (W/L)_2$	$(W/L)_3$	Area (μm^2)
Values Obtained	34.722/3	33.175/3	307.86004
Parameters	Rbias (MΩ)	I_{D1} (μA)	Vout (V)
SPICE Results	120.657	12.657	-2.435

- Differential Pair

Specifications	gmi (μmhos)	Rdp (MΩ)	Id1 (μA)
Values	80	9.26445	15
Topologies available	SDP	CDP	
Gmi obtained (μmhos)	167	167	
Rdp obtained (MΩ)	1.5873	20.996054	
Topologies possible	X	Yes	
Function value		-1.2923	
Final topology selected	Cascode Differential Pair (CDP)		
Device Parameters	$(W/L)_1=(W/L)_2$	$(W/L)_3=(W/L)_4$	Area (μm^2)
Values Obtained	138.88/3	33.175/3	833.33
Parameters	gmi (μmhos)	I_{D1} (μA)	Rdp (MΩ)
SPICE Results	158.936	13.164	46.7181

- Trans Conductance Amplifier

Specifications	gmg (μmhos)	Rog (MΩ)	Rol (MΩ)	Id5 (μA)	Vomax (V)	Vomin (V)
Values	59	1.5806	39.648	20	4.00	-4.00
Topologies available	SGSL	SGCL		CGSL	CGCL	
gmg obtained (μmhos)	111	111		111	111	
Rog obtained (MΩ)	21.739	21.739		65.63	65.63	
Rol obtained (MΩ)	47.619	78.735		47.619	78.735	

Topologies possible	X	Yes	X	Yes
Function value		-4.7614		-8.197
Final Topology selcted	Cascode Gain Cascode Load (CGCL)			
Parameters	$(W/L)_1 = (W/L)_2$	$(W/L)_3 = (W/L)_4$	Area (μm^2)	
Values	23.1481/3	46.2965/3	416.6651	

Parameters	gmg (μmhos)	Rog (MΩ)	Rol (MΩ)	Id5 (μA)	Vomin	Vomax
SPICE results	95.415	105.41	115.532	18.561	4.11	-4.15

- Overall spice simulation results

Variables	Av	CMRR	UGF (MHz)	PM (degree)	Vomax	Vomin
Spice results	7000	$27x10^3$	1.75	53.4^0	4.11	-4.15

The final topology of the designed 2 stage Miller Compensated op amp is made up of the following building sub blocks:

Simple Current Mirror Load

Wilson Current Mirror Bias

Cascode Differential Pair

Transconductance amplifier with Cascode gain and cascode load stage.

The topology generated is shown in Fig: 4.5

Experiment 3

Input Specs	Av	CMRR	SR (V/μs)	Pd (mw)	UGF (MHz)	PM (degree)	Vomax (V)	Vomin (V)
Values	$2.5X10^5$	$10X10^6$	15	1.9	1	75^o	3.75	-3.75

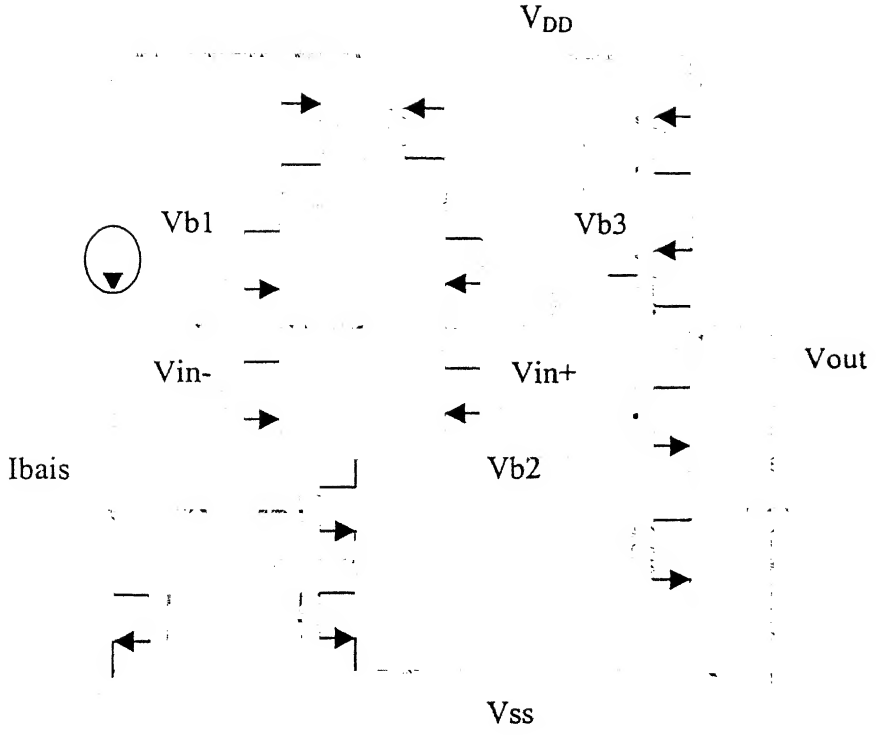

Fig 4.5 Topology generated from Experiment 2

After translation of input specifications using GA into constraints for the sub blocks::

Specs	Rcml (MΩ)	Rbias (MΩ)	Rdp (MΩ)	Rog (MΩ)	Rol (MΩ)	gmi (μmho)	Gmg (μmho)
Values Obtained	73.096	43.5806	5.0645	81.7096	56.0997	41	43

Specs	Av	CMRR	UGF (MHz)
Values obtained	277748.718	10259757.00	1.302828

Topology selection:

- Current Mirror Load

Specifications	Rcml (MΩ)	I_{D1} (μA)	Vomin (Volts)
Value specified	73.096	10	3.4
Topologies	SCM	CCM	WCM

Available			
Rcml obtained (MΩ)	43.475	176.879	264.723
Topologies Possible	X	Yes	Yes
Function value		0.560413	0.310661
Topology Selected	Wilson Current Mirror (WCM)		
Device Parameters	$(W/L)_1$= $(W/L)_2$	$(W/L)_3$	Area (μm^2)
Values Obtained	23.1481/3	22.5718/3	206.604
Parameters	Rcml (MΩ)	I_{D1} (μA)	Vout (V)
SPICE Results	147.819	11.243	3.15

- Current Mirror Bias

Specifications	Rbias (MΩ)	I_{D1} (μA)	Vomin (Volts)
Value specified	43.5806	10	2.15
Topologies Available	SCM	CCM	WCM
Rbias obtained (MΩ)	9.523	54.698	83.651
Topologies Possible	X	Yes	Yes
Function value		-0.336607	-0.271248
Topology Selected	Cascode Current Mirror (CCM)		
Device Parameters	$(W/L)_1$= $(W/L)_2$	$(W/L)_3$	Area (μm^2)
Values Obtained	23.148/3	22.117/3	205.24003
Parameters	Rbias (MΩ)	I_{D1} (μA)	Vout (V)
SPICE Results	171.7618	8.657	-2.71

- Differential Pair

Specifications	gmi (μmhos)	Rdp (MΩ)	Id1 (μA)
Values	41	5.0645	10
Topologies available	SDP	CDP	
gmi obtained (μmhos)	111	111	

Rdp obtained (MΩ)	2.380592	31.49407	
Topologies possible	X	Yes	
Function value		-2.71636	
Final topology selected	Cascode Differential Pair		
Device Parameters	$(W/L)_1=(W/L)_2$	$(W/L)_3=(W/L)_4$	Area (μm^2)
Values Obtained	92.592/3	22.117/3	555.5657
Parameters	gm (μmhos)	I_{D1} (μA)	Rdp (MΩ)
SPICE Results	127.6379	11.146	20.871

- Trans Conductance Amplifier

Specifications	gmg (μmhos)	Rog (MΩ)	Rol (MΩ)	Id5 (μA)	Vomax (V)	Vomin (V)
Values	43	81.7096	56.0997	15	3.75	-3.75

Topologies available	SGSL	SGCL	CGSL	CGCL
gmg obtained (μmhos)	83	83	83	83
Rog obtained (MΩ)	28.985	28.985	87.516	87.516
Rol obtained (MΩ)	63.49	104.98	63.49	104.98
Topologies possible	X	X	Yes	Yes
Function value			-0.57811	-0.80902

Final Topology selcted	Cascode Gain Cascode Load (CGCL)					
Parameters	$(W/L)_1=(W/L)_2$		$(W/L)_3=(W/L)_4$		Area (μm^2)	
Values	17.3611/3		34.7225/3		312.5000	
Parameters	gmg	Rog	Rol (MΩ)	Id5 (μA)	Vomin	Vomax

	(μmhos)	(MΩ)				
SPICE results	64.728	79.161	217.23	13.819	4.05	-3.81

- Overall spice simulation results

Variables	Av	CMRR	UGF (MHz)	PM (degree)	Vomax	Vomin
Spice results	10000	$77x10^4$	0.5	63.4^0	4.05	-3.81

The final topology of the designed 2 stage Miller Compensated op amp is made up of the following building sub blocks:

Wilson Current Mirror Load

Cascode Current Mirror Bias

Cascode Differential Pair

Transconductance amplifier with Cascode gain and Cascode load stage.

It is shown in Fig 4.6

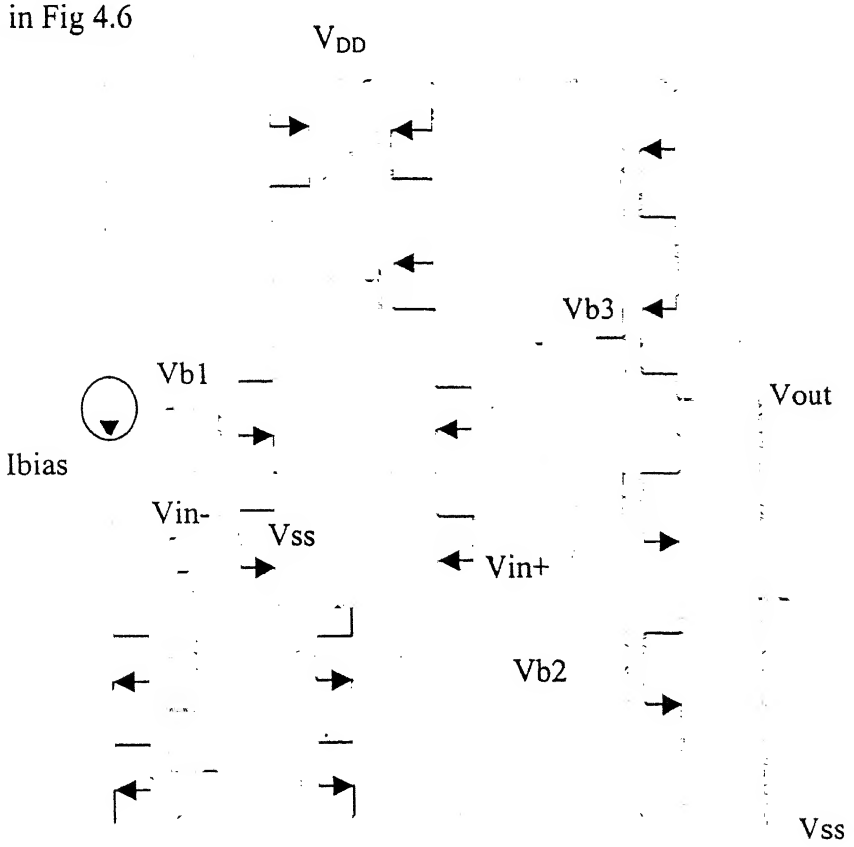

Fig 4.6 Topology generated from Experiment 3

Experiment 4

Input Specs	Av	CMRR	SR (V/μs)	Pd (mw)	UGF (MHz)	PM (degree)	Vomax (V)	Vomin (V)
Values	$19X10^3$	$81X10^4$	25	1.7	1.5	85°	3.85	-3.85

After translation of input specifications using GA into constraints for the sub blocks::

Specs	Rcml (MΩ)	Rbias (MΩ)	Rdp (MΩ)	Rog (MΩ)	Rol (MΩ)	gmi (μmho)	gmg (μmho)
Values Obtained	28.58	4.87096	0.48370	15.2258	39.648	56	73

Specs	Av	CMRR	UGF (MHz)
Values obtained	19431.626	813310.16	1.77947

Topology selection:

- Current Mirror Load

Specifications	Rcml (MΩ)	I_{D1} (μA)	Vomin (Volts)
Value specified	28.58	10	3.5
Topologies Available	SCM	CCM	WCM
Rcml obtained (MΩ)	43.478	176.879	264.723
Topologies Possible	Yes	Yes	Yes
Function value	0.0682	0.090930	0.031264
Topology Selected	Wilson Current Mirror (WCM)		
Device Parameters	$(W/L)_1 = (W/L)_2$	$(W/L)_3$	Area (μm^2)
Values Obtained	22.141/3	22.5714/3	206.60543

Parameters	Rcml (MΩ)	I_{D1} (μA)	Vout (V)
SPICE Results	289.617	9.1911	3.18

- Current Mirror Bias

Specifications	Rbias (MΩ)	I_{D1} (μA)	Vomin (Volts)
Value specified	4.87096	10	2.15
Topologies Available	SCM	CCM	WCM
Rbias obtained (MΩ)	9.523	54.698	83.651
Topologies Possible	Yes	Yes	Yes
Function value	-0.51837	-5.094009	-8.57245
Topology Selected	Wilson Current Mirror (WCM)		
Device Parameters	$(W/L)_1=(W/L)_2$	$(W/L)_3$	Area (μm^2)
Values Obtained	23.1481/3	22.117/3	205.24
Parameters	Rbias (MΩ)	I_{D1} (μA)	Vout (V)
SPICE Results	178.353	9.156	- 2.845

- Differential Pair

Specifications	gmi (μmhos)	Rdp (MΩ)	Id1 (μA)
Values	56	0.4837	10
Topologies available	SDP		CDP
gmi obtained (μmhos)	111		111
Rdp obtained (MΩ)	2.38095		31.49407
Topologies possible	Yes		Yes
Function value	-1.95110		-9.3568
Final topology selected	Cascode Differential Pair		
Device Parameters	$(W/L)_1=(W/L)_2$	$(W/L)_3=(W/L)_4$	Area (μm^2)

Values Obtained	23.148/3	22.117/3	271.5911
Parameters	gmi (μmhos)	I_{D1} (μA)	Rdp (MΩ)
SPICE Results	102.6379	9.146	172.871

- Trans Conductance Amplifier

Specifications	gmg (μmhos)	Rog (MΩ)	Rol (MΩ)	Id5 (μA)	Vomax (V)	Vomin (V)
Values	73	15.2258	39.648	25	3.85	-3.85

Topologies available	SGSL	SGCL	CGSL	CGCL
gmg obtained (μmhos)	139	139	139	139
Rog obtained (MΩ)	17.391	17.391	52.5012	52.5012
Rol obtained (MΩ)	38.095	62.988	38.095	62.988
Topologies possible	X	Yes	X	Yes
Function value	____	-0.759317	____	-1.153301

Final Topology selcted	Cascode Gain Cascode Load (CGCL)		
Parameters	$(W/L)_1 = (W/L)_2$	$(W/L)_3 = (W/L)_4$	Area (μm^2)
Values	28.935/3	57.8703/3	520.83313

Parameters	gmg (μmhos)	Rog (MΩ)	Rol (MΩ)	Id5 (μA)	Vomin	Vomax
SPICE results	117.18	71.819	117.617	22.718	3.871	-4.18

- Overall spice simulation results

Variables	Av	CMRR	UGF (MHz)	PM (degree)	Vomax	Vomin

Spice results	9000	$31x10^3$	1.25	73.4^0	3.871	-4.18

The final topology of the designed 2 stage Miller Compensated op amp is made up of the following building sub blocks:

Wilson Current Mirror Load

Wilson Current Mirror Bias

Cascode Differential Pair

Transconductance amplifier with Cascode gain and Cascode load stage.

It is shown if Fig 4.7

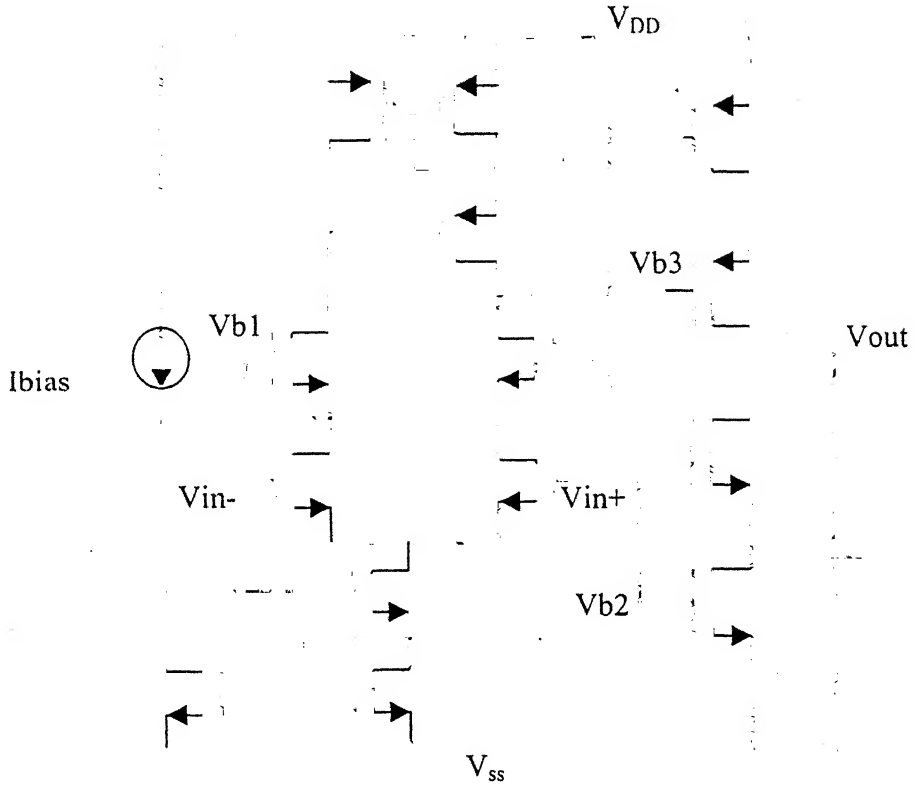

Fig 4.7 Topology generated from Experiment 4

Experiment 5

Input Specs	Av	CMRR	SR (V/μs)	Pd (mw)	UGF (MHz)	PM (degree)	Vomax (V)	Vomin (V)
Values	$10X10^4$	$30X10^6$	5	0.7	3	3	4.44	-4.44

After translation of input specifications using GA into constraints for the sub blocks::

Specs	Rcml (MΩ)	Rbias (MΩ)	Rdp (MΩ)	Rog (MΩ)	Rol (MΩ)	gmi (μmho)	gmg (μmho)
Values Obtained	49.096	34.677	6.811	81.7890	11.0557	97	19

Specs	Av	CMRR	UGF (MHz)
Values obtained	107413.351	30492882.78	3.082

Topology selection:

- Current Mirror Load

Specifications	Rcml (MΩ)	I_{D1} (μA)	Vomin (Volts)
Value specified	49.096	20	3.69
Topologies Available	SCM	CCM	WCM
Rcml obtained (MΩ)	63.475	176.879	264.723
Topologies Possible	X	X	X
Function value			
Topology Selected	Design not feasible (conflicting specs)		
Device Parameters	$(W/L)_1 = (W/L)_2$	$(W/L)_3$	Area (μm^2)
Values Obtained			
Parameters	Rcml (MΩ)	I_{D1} (μA)	Vout (V)
SPICE Results			

- Current Mirror Bias

Specifications	Rbias (MΩ)	I_{D1} (μA)	Vomin (Volts)
Value specified	34.6777	20	2.15
Topologies	SCM	CCM	WCM

Available			
Rbias obtained (MΩ)	4.761	27.349	41.825
Topologies Possible	X	X	Yes
Function value			0.118372
Topology Selected	Wilson Current Mirror (WCM)		
Device Parameters	$(W/L)_1 = (W/L)_2$	$(W/L)_3$	Area (μm^2)
Values Obtained	46.296/3	44.234/3	410.48007
Parameters	Rbias(MΩ)	I_{D1} (μA)	Vout (V)
SPICE Results	79.17891	18.975	-2.189

- Differential Pair

Specifications	gmi (μmhos)	Rdp (MΩ)	Id1 (μA)
Values	97	6.8111	20
Topologies available	SDP	CDP	
gmi obtained (μmhos)	222	222	
Rdp obtained (MΩ)	1.190476	15.747039	
Topologies possible	X	Yes	
		-1.65333	
Final topology selected	Cascode Differential Pair (CDP)		
Device Parameters	$(W/L)_1 = (W/L)_2$	$(W/L)_3 = (W/L)_4$	Area (μm^2)
Values Obtained	185.18/3	44.234/3	1111.1617
Parameters	gmi (μmhos)	I_{D1} (μA)	Rdp (MΩ)
SPICE Results	264.819	22.146	10.716

- Trans Conductance Amplifier

Specifications	Gmg (μmhos)	Rog (MΩ)	Rol (MΩ)	Id5 (μA)	Vomax (V)	Vomin (V)
Values	19	81.7890	11.0557	5	4.44	-4.44

Available			
Rbias obtained (MΩ)	4.761	27.349	41.825
Topologies Possible	X	X	Yes
Function value			0.118372
Topology Selected	Wilson Current Mirror (WCM)		
Device Parameters	$(W/L)_1 = (W/L)_2$	$(W/L)_3$	Area (μm^2)
Values Obtained	46.296/3	44.234/3	410.48007
Parameters	Rbias(MΩ)	I_{D1} (μA)	Vout (V)
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SPICE Results	264.819	22.146	10.716

- Trans Conductance Amplifier

Specifications	Gmg (μmhos)	Rog (MΩ)	Rol (MΩ)	Id5 (μA)	Vomax (V)	Vomin (V)
Values	19	81.7890	11.0557	5	4.44	-4.44

Topologies available	SGSL	SGCL	CGSL	CGCL
gmg obtained (μmhos)	28	28	28	28
Rog obtained (MΩ)	86.956	86.956	262.549	262.549
Rol obtained (MΩ)	190.476	314.940	190.476	314.940
Topologies possible	Yes	Yes	X	X
Function value	-2.16781	-3.0467		
Final Topology selcted	Simple Gain Cascode Load (SGCL)			

Parameters	$(W/L)_1$	$(W/L)_3 = (W/L)_2$	Area (μm^2)
Values	5.78703/3	11.574/3	86.8055

Parameters	Gmg (μmhos)	Rog (MΩ)	Rol (MΩ)	Id5 (μA)	Vomin	Vomax
SPICE results	23.711	171.181	514.516	4.817	4.81	-4.81

The final topology of the designed 2 stage Miller Compensated op amp couldn't be designed because of conflicting parameters.

Experiment 6

Input Specs	Av	CMRR	SR (V/μs)	Pd (mw)	UGF (MHz)	PM (degree)	Vomax (V)	Vomin (V)
Values	$40X10^4$	$30X10^6$	20	1.6	3	70	3.91	-3.91

After translation of input specifications using GA into constraints for the sub blocks::

Specs	Rcml (MΩ)	Rbias (MΩ)	Rdp (MΩ)	Rog (MΩ)	Rol (MΩ)	gmi (μmho)	gmg (μmho)
Values Obtained	49.0967	34.677	9.293	46.096	12.375	97	59

Specs	Av	CMRR	UGF(MHz)
Values obtained	436311.844	30049818.47	3.082

Topology selection:

- Current Mirror Load

Specifications	Rcml (MΩ)	I_{D1} (μA)	Vomin (Volts)
Value specified	49.0967	20	3.56
Topologies Available	SCM	CCM	WCM
Rcml obtained (MΩ)	53.7819	88.4396	132.361
Topologies Possible	Yes	X	X
Function value	0.077787		
Topology Selected	Simple Current Mirror (SCM)		
Device Parameters	$(W/L)_1$	$(W/L)_2$	Area (μm^2)
Values Obtained	23.141/3	23.141/3	214.617
Parameters	Rcml (MΩ)	I_{D1} (μA)	Vout (V)
SPICE Results	87.242	17.781	-3.181

- Current Mirror Bias

Specifications	Rbias (MΩ)	I_{D1} (μA)	Vomin (Volts)
Value specified	34.677	20	2.15
Topologies Available	SCM	CCM	WCM

Rbias obtained (MΩ)	4.7619	27.349	41.825
Topologies Possible	X	X	Yes
Function value			0.113192
Topology Selected	Wilson Current Mirror (WCM)		
Device Parameters	$(W/L)_1 = (W/L)_2$	$(W/L)_3$	Area (μm^2)
Values Obtained	46.296/3	44.234/3	410.48007
Parameters	Rbias (MΩ)	I_{D1} (μA)	Vout (V)
SPICE Results	167.6718	18.758	-2.981

- Differential Pair

Specifications	gmi (μmhos)	Rdp (MΩ)	Id1 (μA)
Values	97	9.293	20
Topologies available	SDP		CDP
gmi obtained (μmhos)	222		222
Rdp obtained (MΩ)	1.19047		15.747089
Topologies possible	X		Yes
Function value			
Final topology selected	Cascode Differential Pair (CDP)		
Device Parameters	$(W/L)_1 = (W/L)_2$	$(W/L)_3 = (W/L)_4$	Area (μm^2)
Values Obtained	185.185/3	44.234/3	1111.1096
Parameters	gmi (μmhos)	I_{D1} (μA)	Rdp (MΩ)
SPICE Results	217.6351	19.146	27.871

- Trans Conductance Amplifier

Specifications	Gmg (μmhos)	Rog (MΩ)	Rol (MΩ)	Id5 (μA)	Vomax (V)	Vomin (V)
Values	59	46.096	12.375	20	3.91	-3.91
Topologies	SGSL	SGCL	CGSL	CGCL		

available				
gmg obtained (μmhos)	111	111	111	111
Rog obtained (MΩ)	21.731	21.731	65.6347	65.6347
Rol obtained (MΩ)	47.619	78.735	47.619	78.735
Topologies possible	X	Yes	X	Yes
Function value		-2.78494		-1.573589

Final Topology selcted	Simple Gain Cascode Load (SGCL)

Parameters	$(W/L)_1$	$(W/L)_3 = (W/L)_2$	Area (μm^2)
Values	23.1481/3	46.296/3	416.66

Parameters	Gmg (μmhos)	Rog (MΩ)	Rol (MΩ)	Id5 (μA)	Vomin	Vomax
SPICE results	91.252	54.9171	117.6717	17.415	3.617	-4.12

- Overall spice simulation results

Variables	Av	CMRR	UGF (MHz)	PM (degree)	Vomax	Vomin
Spice results	15000	$27x10^5$	2.15	73.4^0	3.171	-4.12

The final topology of the designed 2 stage Miller Compensated op amp is made up of the following building sub blocks:

Simple Current Mirror Load

Wilson Current Mirror Bias

Cascode Differential Pair

Transconductance amplifier with Simple gain and Cascode load stage.

It is shown in Fig 4.8

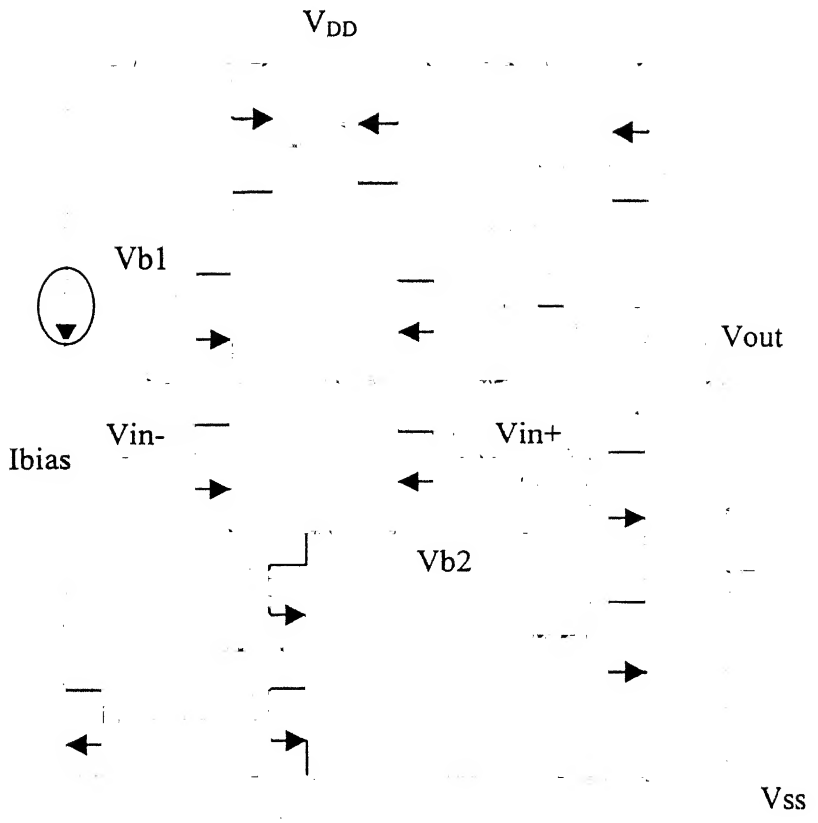

Fig 4.8Topology generated from Experiment 6

CHAPTER 5

CONCLUSIONS AND SUGGESTIONS

It is a well known fact that optimization at the top most level of a hierarchical framework of design yields the maximum gain in terms of performance parameters. Thus if we are able to generate an optimized topology at the top most level then we can expect to get the best performance.

In this work we have presented a framework to support behavior to structure synthesis of analog circuits. This framework relies on a hierarchical representation of circuits. Initially it chooses a particular design style from among a set of fixed design styles at the top most level of the hierarchy. Initially, a particular topology to be designed is selected at the top most level of the hierarchy. This is followed by a design phase where the input specifications are translated from the top most level in the hierarchy to the next lower, more concrete level. Genetic Algorithm based optimization is used during this translation process to obtain the new optimized set of specifications for each of the building sub blocks. The specifications obtained for each sub block are divided into two sets S_0 and S_1. One subset of the specs (S_0) along with the choice of a topology is used to generate a new value for the other subset S_1'. Depending on the match between the elements of S_1 and S_1' the topology is considered a success or a failure. Final topology is selected from among the successful topologies using a suitable figure of merit. The validity of this approach is demonstrated by designing several kinds of 2 stages Miller Compensated op amp which is an affixed connection of different building sub blocks such as load current mirrors, differential pairs, bias current mirrors and trans conductance amplifiers.

Suggestion for Future Works

The following modifications and additions are required to make a complete synthesis tool which can be easily handled by an inexperienced designer.

- Interfacing the circuit simulation tool, e.g. SPICE that will enable the designer to simulate and verify the design simultaneously.
- Demonstrate the methodology on more complex analog circuits e.g., the phase-locked loop (PLL), the switched capacitor filter etc, translation of the input specs have to be done to obtain performance constraints for the building sub blocks.
- Interfacing of layout generation tools, in order to generate the layout of the circuit and subsequently, optimization can be performed taking into account the exact parasitic capacitances obtained from the layout of the circuit.
- Building an interface with the symbolic circuit simulator e.g., ISSAC or SAPWIN [16] which will provide the analytical equations required for topology selection.
- Finally a tool must be developed which can automate the initial top most level design style selection operation to obtain a more efficient and effective automated design process.

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APPENDIX I

The MOS Technology File

A set of process parameters for typical silicon- gate n-well CMOS process with 3μm technology, which has been used in this work of generating the overall topology of a 2 stage Miller compensated op amp is given below:

Sr. No.	Parameter	Symbol	*Value*	
			n-channel	*p-channel*
1.	Substrate doping (atoms/cm^3)	N_A, N_D	1x10^{15}	1x10^{16}
2.	Gate oxide thickness (A^o)	t_{ox}	400	400
3.	Metal-silicon work function (V)	φ_{ms}	-0.7	-0.1
4.	Channel mobility (cm^2/V-sec)	μ_n, μ_p	700	350
5.	Minimum drawn channel length (μm)	L_{drawn}	3	3
6.	Source, drain junction depth (μm)	X_j	0.6	0.6
7.	Source, drain side diffusion (μm)	L_d	0.3	0.3
8.	Overlap capacitance per unit gate width (fF/μm)	C_{ol}	0.35	0.35
9.	Threshold adjust effective depth (μm)	X_i	0.3	0.3

10.	Threshold adjust effective surface concentration (atoms/cm^3)	N_{si}	$2x10^{16}$	$0.9x10^{16}$
11.	Nominal threshold voltage (V)	V_t	0.75	0.75
12.	Poly silicon gate doping concentrations (atoms/cm^3)	N_{dpoly}	10^{20}	10^{20}
13.	Poly gate sheet resistance ($\Omega/\square$)	R_s	20	20
14.	Source / drain-bulk junction capacitance per unit source/drain area (fF/μm^2)	C_{jo}	0.08	0.20
15.	Source /drain bulk junction capacitance grading coefficient	n	0.5	0.5
16.	Source / drain periphery capacitance per unit source drain periphery (fF/μm)	C_{jswo}	0.5	0.5
17.	Source/drain- periphery capacitane grading coefficient	n	0.5	0.5
18.	Source, drain junction built-in potential (V)	φ_o	0.65	0.65
19.	Surface state density (atoms/cm^3)	N_{ss}	10^{11}	10^{11}
20.	Channel length modulation parameter (μ/V)	dX_d/dV_{DS}	0.2	0.1

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